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POLYSILICON AMLCD PROJECTOR

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13. ABSTRACT *(Maximum 200 words)*

A polysilicon thin film transistor (TFT) echnology integrated with information of a light shield and a pixel electrode was transferred to a commercial integrated circuit foundry and was demonstrated to be optimized for manufacturing by successful fabrication of 1280 x 1024 prototype displays. Transmission and contrast ratio values suitable for a projection light valve were achieved.

The 1280 x 1024 display was designed for optimum performance with the polysilicon TFT technology. Design-for-test features were included to permit wafer-level evaluation and repair. A detailed description of the design by block, including multiplexer, sample/hold, data driver, select scanner, and timing functions, was documented. A detailed set of specifications, including electrical characteristics, timing diagrams, optical characteristics, suggested operating procedures, and pin assignments, were defined.

A complete process flow that integrates an ITO technology and topographical planarization with the underlying transistor architecture was demonstrated to be fully compatible with commercial integrated circuit manufacturing facilities. In addition, an efficient, manufacturing-ready technology to introduce hydrogen into TFTs for achievement of optimum on-and off-state characteristics was achieved. Key requirements for high-yield manufacturing of the light valves were identified.

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1.0 PROGRAM OVERVIEW

The work reported here focused on demonstration of a factory-producible, polysilicon, thin-film-transistor technology suitable for manufacturing of a 1280 x 1024 light valve in support of the goals of the Polysilicon AMLCD Projector Program. The technical achievements are part of a continuing effort whose initial results can be found in a previous report, WL-TR-95-1163. The key objectives of the effort summarized in this report were optimization of the process technology, specification of the equipment requirements for manufacturing, development of the design and specifications for the light valve, and definition of acceptable device parametrics.

As a result of the work performed, a fully qualified process technology was transferred to a commercial foundry and demonstrated by successful fabrication of devices. Process optimization efforts described in this report focused on the back end of the flow, including an indium-tin-oxide (ITO) technology and the Sarnoff hydrogenation system for device passivation. The front end of the process sequence was previously described in the above referenced report. Design of the 1280 x 1024 was accomplished and light valves were fabricated and tested. Measurements demonstrate that optical performance suitable for a projection system light valve was achieved.

2.0 PROGRAM ACCOMPLISHMENTS

The effort described in this report resulted in a process technology suitable for manufacturing in a standard integrated circuit facility and in functioning 1280 x 1024 light valves made with the technology. Specifically demonstrated were:

- A 1280 x 1024 display design with preliminary specifications.
- Fabricated 1280 x 1024 light valves with measured transmission and contrast ratio suitable for a projection light valve.
- A complete process flow, fully compatible with commercial integrated circuit manufacturing facilities, that integrates an ITO technology with adequate topographical planarization for pixel electrodes.
- An efficient, manufacturing-ready technology to introduce hydrogen into TFTs for achievement of optimum on- and off-state characteristics.
- Specification of equipment for manufacturing.
- Device parametric requirements to achieve designed light valve performance.

3.0 DISPLAY WAFER PROCESSING

3.1 Introduction

A previous report, WL-TR-95-1163, described in detail the front-end process flow for fabrication of TFTs in polysilicon. As discussed there, the Sarnoff technology was developed to be compatible with a conventional, high-volume MOS production facility. Validation was accomplished by successful demonstration of devices that were fabricated in a commercial foundry.

Subsequent to polysilicon TFT fabrication and definition of the black matrix material, the final display wafer is produced by addition of the pixel electrode material and an overcoat followed by a hydrogenation process to optimize transistor characteristics by passivation of the active-area material. In Section 3.2 below, the ITO and overcoat process sequence are described, with emphasis on key aspects relevant to process control. All of the unit step operations are compatible with standard integrated circuit processing facilities.

A hydrogenation process, described below in Section 3.3, is essential to achieve low leakage and high drive currents in polysilicon transistors, thus producing optimized circuit performance. The hydrogenation process developed by Sarnoff is done after all other wafer processing steps are completed, thus allowing flexibility in choice of manufacturing facilities, with options for establishment of the process flow with or without the final passivation in a foundry. The hydrogenation process can be done with equipment compatible with standard handling tools for semiconductor wafers and provides very rapid introduction of hydrogen into the TFT device structure.

3.2 MOS-ITO Process Integration

The 1280 x 1024 display technology employs transparent pixel electrodes to achieve a high transmission display. The electrodes are formed from indium tin oxide (ITO). The process steps for incorporation of the ITO pixel electrodes after black matrix patterning are described below and a schematic of the process flow is provided by Figure 3-1. Unit steps involved are planarization, inter-level dielectric deposition, ITO contact formation, ITO deposition, ITO patterning, overcoat deposition, and overcoat patterning. Although not a part of conventional semiconductor processing, ITO preparation and etching differ little from the types of unit step operations associated with integrated circuit fabrication.

3.2.1 Topography Planarization

Planarization of the topography surrounding the pixel area is key to achievement of a device architecture for yield and reliability. The definition of active-area polysilicon, gate polysilicon, metal-1, and black matrix material all contribute to produce a variety of step heights and contours at different locations within the circuit. Planarization is needed to ensure that the ITO layer is continuous over steps and that the pixel electrode has small contour irregularities, thus minimizing undesirable optical effects in the liquid crystal material at high field regions.

A spin-on glass (SOG) planarization procedure is used to eliminate steep steps that exist after definition of the black matrix material over the first deposited-oxide isolation layer. The SOG film is applied directly to the black matrix and the dielectric over metal-1. A partial planarization by plasma etching is done before deposition of the inter-level dielectric (ILD) layer. At this point in the process, various layers are exposed, but the topological features have contours favorable to achieve good coverage with overlying films.

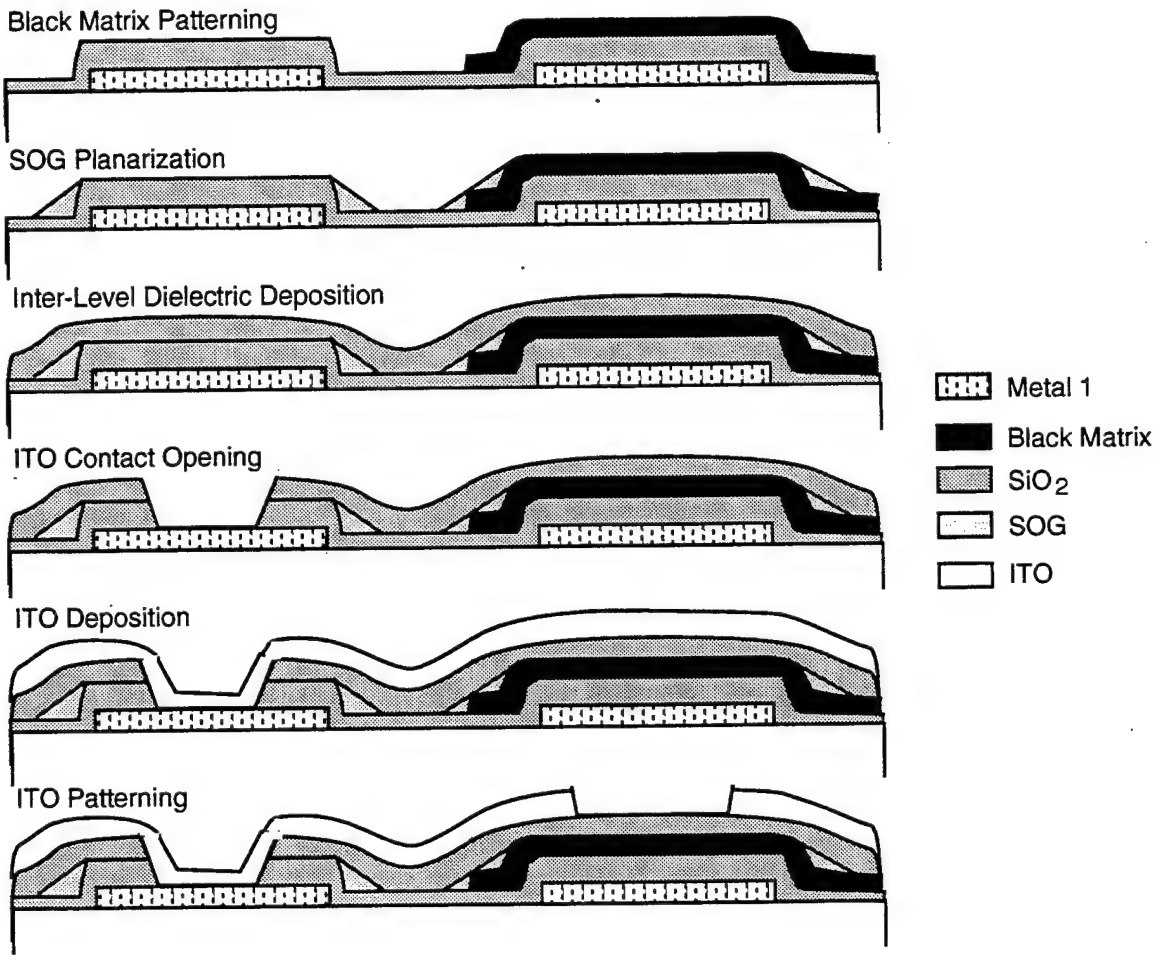


Figure 3-1. Architectural schematic for wafer above TFTs.

3.2.2 Inter-Level Dielectric Deposition

The inter-level dielectric isolates the ITO pixel electrodes from the black matrix layer, which is coincident with the ITO pixel on two sides of each pixel cell. The interlevel dielectric is typically a plasma-enhanced oxide (PEO), which is deposited at a low temperature, less than 400°C, and is a transparent and compressively-stressed film. An appropriate film thickness for effective ITO isolation from the black matrix is 400 nm.

3.2.3 ITO Contact Formation

In display operation, the ITO pixel electrode is biased by a contact to metal-1. The formation of this contact cut is done through the two deposited oxide layers, each approximately 400 nm thick. The ITO must be continuous into the contact opening and make good electrical contact to the aluminum metallization. Since the nominal ITO film thickness is only 120 nm, thinning into the contact opening must be minimized. Hence, it is desirable that the ITO contact opening be smooth and well-tapered down to metal-1. The typical contact resistance for a single ITO to metal contact is 500 to 1000 Ω. Contacts made to aluminum require processing conditions that ensure adequate contact resistance for all ITO contacts.

3.2.4 ITO Deposition

A thin film of ITO is deposited on the wafer to provide a transparent electrode at each pixel. Minimum requirements on the electrode material for the process as defined during the program are:

- maximum light transmission, at least 84%, in the visible
- suitably low resistance, ≈ 50-200 Ω/sq for a 100-nm film
- etchable without significant attack of other exposed materials.

In general, the properties of ITO are system and process sensitive. There are as many ITO process recipes as types of deposition systems and ITO target formulations. For the program, ITO was deposited by low-power dc magnetron sputtering in an Innotec 14-ILS in-line system under an argon atmosphere. The target was a moderately dense, approximately 80% of theoretical, 10% tin oxide target supplied by Tosoh, Inc. Deposition was done at 400 W, which corresponds to an average power density of 0.62 W/cm^2; under this condition the temperature rise of the substrate is almost nil.

The as-deposited films have a transmission in the range 70-80% and sheet resistance near 150-250 Ω/sq. A short air bake at 180-195°C for 30-60 minutes increases the optical transmission to 83-85% and reduces the resistance to 30-50 Ω/sq. The bake cycle is that normally done to process photoresist used to pattern the ITO, so that no special additional heat treatment is required.

The ITO prepared as described is easily etched in a standard HCl-based solution after photolithographic definition.

3.2.5 ITO Patterning

After deposition the ITO is patterned employing conventional positive resist processing and wet chemical etching. The ITO etch attacks aluminum readily and it is essential that no aluminum be exposed during the wet etch. No pinholes in the inter-level dielectric can exist, and the adhesion of the resist to the ITO must be good to minimize undercutting. The etch rate must also be optimized: short etch times, less than 30 s, provide inadequate process control and excessively long etch times attack and ultimately lift the resist.

A number of process tests were done to optimize the wet ITO etch procedure. The tests included investigation of etchant composition, etchant temperature, use of various adhesion pre-treatments, and use of various ITO cure conditions. Since the ITO films are transparent, the time to etch the film is difficult to determine visually. A conductivity probe was used to determine the endpoint of the etch.

Figure 3-2 shows etch times for the ITO patterning runs done with a fixed wet-etch process. The uniformity of the etch times within a deposition run and across a wafer was good. However, there was considerable variability in the etch times among the depositions, due presumably to slight differences in composition, as thickness variations were small. An ITO control wafer was used for every deposition run to determine the etch time of the device wafers in a lot. The time period covered by the 16 deposition runs is almost eight months. An etch time of about 1 min appears to be correct for the final process. It is anticipated that better control of composition and etch times will be achieved in a high-volume production environment than was found with the development lots.

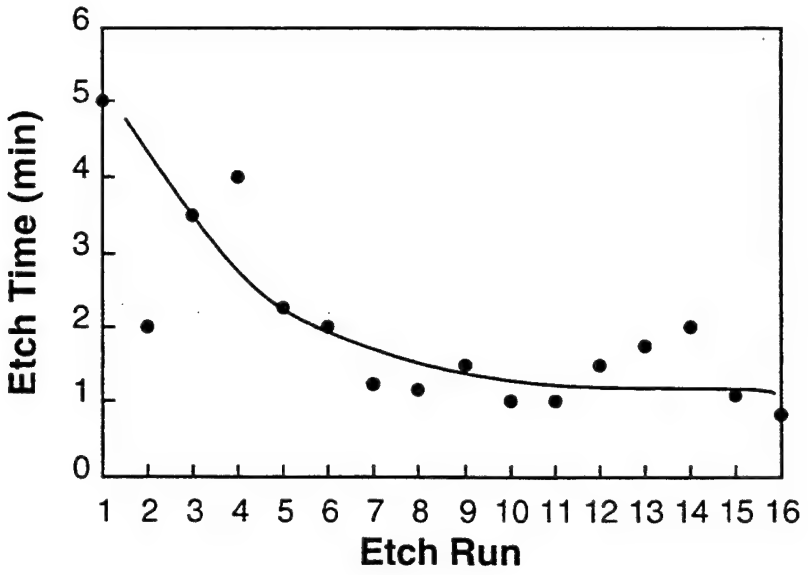


Figure 3-2. Summary of ITO etch tests for definition of optimized etch process.

3.2.6 Overcoat Deposition and Bond Pad Etch

The final step of the process flow is deposition of a protective oxide layer, nominally 300 nm thick, for the device. Either a plasma-deposited oxide similar to the inter-level dielectric or a CVD-deposited oxide can be used. The bond pad openings through the various deposited oxide layers are patterned with a single photoresist and etch step.

3.3 Hydrogenation

Passivation of thin film polysilicon transistors by introduction of hydrogen is a key process that produces substantial improvements in device parameters such as off-state leakage current and on-state drive current. Two types of hydrogenation techniques have been described in the literature: one uses thermally activated transfer from a hydrogen-rich material such as silicon nitride and the other involves exposure to a hydrogen species generated with a plasma source. While the exact mechanism of these hydrogenation processes is not well understood, it is presumed that the improvement in transistor performance is due to passivation of defects in the polysilicon, especially at grain boundary sites.

Our experience has shown that a saturated passivation effect with a wide window of system parameters can be efficiently achieved with a remote downstream plasma system. In contrast, times on the order of hours are typically reported to be required to achieve a significant effect. The Sarnoff process is therefore more adaptable for production purposes and was used exclusively during the program.

3.3.1 Hydrogenation System

A plasma system designed and built for transistor hydrogenation was used for passivation of the polysilicon TFTs. The main system chamber is an 18" x 30" metal bell jar. Facility is made for convenient insertion and removal of wafers through a port. The system is equipped with a diffusion-based pumping system capable of providing an operational pressure below 1E-4 torr. Various gases, including hydrogen, helium, and nitrogen, can be introduced into the system.

The processed wafer, after formation of the TFT structure and top layers, is placed on a substrate remote from the plasma source. The heater for this substrate is capable of reaching about 550°C, although temperatures lower than this are employed. Substrate temperature, power, time, and gas mixture are the key parameters that are controlled for operation of the system.

3.3.2 Process Development

The hydrogenation process developed during the program is a refinement of previous work that required hydrogenation of both nMOS and pMOS transistors in polysilicon material. The objective was to develop and demonstrate a production-worthy process to consistently passivate pMOS transistors, for which, in our experience, remote downstream plasma systems have a much wider window of operating parameters than for the case of nMOS devices. Off-state leakage current of pixel transistors is the parameter crucial to successful operation of the light valve: a zero-bias leakage current not exceeding 1 pA/μm in transistors with the pixel device architecture is needed. The system parameters investigated were the substrate temperature, the hydrogenation time, and the hydrogen to helium ratio in the plasma.

The best and most consistent results were obtained when the substrate temperature was 450°C, the helium to hydrogen ratio was 20/1, and the applied power was 600 W. These conditions were adopted as the standard process.

With the final process, high on-state current, high sub-threshold slope, low off-state current, and a nearly ideal threshold voltage were achieved. A detailed database was generated from all passivation runs with the final process, and examples of the data analysis done for transistor parameters are provided in Section 5.4.

4.0 PROCESS EQUIPMENT SPECIFICATIONS

4.1 Introduction

The wafer fabrication technology defined during the program is compatible with standard integrated circuit process equipment, including wafer handling systems. All unit step operations, including ITO processing, can utilize standard factory processing equipment and tools. The hydrogenation equipment, although specially designed for TFT passivation, is also compatible with standard integrated circuit unit step operations and wafer handling procedures.

In the following sections, key aspects of the equipment requirements are summarized. Emphasis is given to providing the important system attributes, rather than on specific equipment recommendations. Numerous vendors can provide equipment appropriate for the various unit step operations.

4.2 ITO Equipment

A primary consideration for the selection of processing equipment is minimization of particulate generation—the overriding concern for manufacture of large displays. Hence, equipment with automated wafer handling is highly desirable to maximize yield. The ability to handle fused silica substrates must be considered. Wafer transparency is probably not an issue, however, since the wafers are coated with aluminum and black matrix material, hence permitting their detection by the optical sensors on wafer handling tools. Processes that rely on heating the wafer with lamps or RF sources are not as effective with silica wafers as are processes employing direct transfer heating. All processes after aluminum metallization are carried out at temperatures less than 400° C.

4.2.1 SOG Coater

Numerous commercial coaters are available for dispensing and curing low particulate SOG material. Most machines feature automatic bowl rinses, dispensed tip cleans, and sequential hot plates for rapid curing of the films.

4.2.2 Plasma-Enhanced Deposition System

Plasma-enhanced deposition systems are available in many varieties. The most important aspect of the deposition is achievement of low levels of particulate contamination. The plasma deposited SiO_2 film should have a low compressive stress. The conformality of the deposited film over steps is not a critical parameter.

4.2.3 Oxide Dry Etcher

The dry oxide etcher is used for several of the unit step operations, including the partial etchback of the SOG for planarization, the etching of tapered ITO contacts, and the final bond pad etch. Again the particulate level is a critical factor for selection of equipment. Single wafer machines might be preferred, because operator handling is minimized.

4.2.4 ITO Deposition System

The sputtering system envisioned for the ITO process should be a manufacturing-ready machine of proven robustness and flexibility. It may be significantly different than the Innotec sputtering system used during the development program. The Varian 3180 system is an example of an appropriate machine for production of display wafers. It is a high throughput, automatically controllable, cassette-to-cassette system of proven reliability over many years. Possible deposition arrangements include a two-target/two-etch station configuration or a three-target/single-etch station configuration. Both set-ups permit the deposition of one-half the desired film thickness at each of two adjacent targets so that high throughput can be achieved. The usual conical magnetron targets may be replaced with planar target assemblies to enable use of high density ceramic ITO targets of the type recently developed by Merck-Balzers and Tosoh, thus achieving a highly repeatable process as well as maximum target utilization.

4.2.5 Temperature-Controlled Wet Etch Station

The wet etch of the ITO film must be done in a temperature controlled bath to provide uniform and reproducible etch times. The etch system must handle both corrosive and oxidizing chemicals such as HCl, HNO_3, H_2SO_4, and H_2O_2. The station should also include a dump rinser to remove chemicals from the substrate surface. The particulate level is key for all aspects of the wet etch processing.

4.2.6 Megasonic Clean Unit

Megasonic cleans are recommended throughout display wafer processing, because they are very effective for the removal of particulate contamination. Because the ITO process follows the aluminum metallization, all cleans are done only in deionized water. It is recommended that a cleaning operation follow every plasma etch, wet etch, or plasma strip operation during the process flow.

4.2.7 Plasma Stripper

All resist removal cycles are done with an oxygen plasma. Lamp or rf heating of the substrate during the resist removal step is probably less effective than direct transfer heating. The particulate level of the stripper is again critical.

4.3 Hydrogenation Equipment

The hydrogenation process used for the passivation of polysilicon TFTs during this program can be done in any vacuum system with a remote downstream plasma source and with the following features:

1. Flow controls to introduce nitrogen, hydrogen, and helium during the process cycle.
2. Pumping capability to achieve a base pressure below about 5E-6 torr.
3. Pumping capability to control pressure below 1E-4 torr at 25 sccm gas flow.
4. System dimensions that permit the distance between the plasma source and the wafer to be at least 12 in.

5. A substrate with a heater to provide control of wafer temperature.

For throughput considerations in a production environment, other features are desirable. Exactly what is needed would depend upon whether the system is designed for batch or single-wafer processing. In the latter case, facility for rapid loading and unloading is important and an efficient means to rapidly cool the wafer in the plasma is needed. A production system meeting all of these requirements can be specified.

5.0 WAFER ACCEPTANCE TEST

5.1 Introduction

Optimized display performance depends upon achievement of good transistor performance. Test structures, as part of a test chip, were designed to permit detailed characterization of all aspects of transistor behavior. These structures include resistors, which measure sheet resistance of various layers; contact resistance devices, which measure the contact resistance of a single contact; and transistors of various geometries that mimic those of the subcircuits in the display. A wafer acceptance test (WAT) procedure suitable for a manufacturing environment was developed and defined.

5.2 Test Structure Description

Below are described all of the special structures that were designed and included on wafers for assessment purposes. Resistors were used to monitor all implants for correct dose. Four-terminal contacts were included to track contact resistance. A variety of transistors were available to monitor key device parameters.

5.2.1 Resistor Monitors

Resistors in the form of a bar are used to measure the sheet resistance, in ohms per square, of all critical layers. The layout is a four terminal device consisting of metal probe pads 200 μm x 200 μm in size connected to 10 squares of the layer being tested. The following sheet resistances are determined:

1) P+ source/drain in active-area polysilicon
2) N+ gate in polysilicon or silicide material
3) P+ capacitor electrode in active-area polysilicon
4) ITO

5) P-type LDD in active-area polysilicon.

5.2.2 Contact Resistance Monitors

Contact resistance structures, consisting of a single 2.5-µm x 2.5-µm contact, are used to monitor contact resistance, in ohms, between metal and other layers. The test structures are designed for Kelvin probing, with a probe pad layout similar to that of the resistance monitors. All contacts in the structures are much larger, 6.0 µm x 6.0 µm, than the one under test. The contact resistance is measured between the following levels:

1) Metal to P+ active-area polysilicon
2) Metal to gate material
3) ITO to metal

5.2.3 Transistor Test Structures

The performance characteristics of key transistors are evaluated at specific bias conditions defined to correlate with how the transistors are used in the display. The structures have four terminals with the same probe pad layout as the other test structures; three of the pads address the gate, the source, and the drain of the transistor and the fourth pad is shorted to the drain pad and used as part of a probes-down test. The contacts are 2.5 µm x 2.5 µm for the pixel transistors and 3.0 µm x 3.0 µm for the other transistors. The transistors and parametrics measured are as follows:

1) Pixel transistors - the pixel transistors, 2.5 µm wide, 4.0 µm long, and with LDDs, are measured with 12 V applied to the drain for the following:
   a) $I_{off\ (minimum)}$ - the minimum leakage current.
   b) I_{off} (V_g=0) - the leakage current with V_g=0, indicating if the device is off.
   c) I_{on} -the drive current at a particular on-state condition.
   d) V_t - the threshold voltage measured with V_d=0.1 V, done before the drain voltage is raised to 12 V to minimize any measurement induced effects.

e) V_{bd} - the drain breakdown voltage, which is defined as the drain voltage at which the source-drain current is 10 μA for zero gate bias.

f) Mobility - the maximum mobility of the transistor, in $cm^2/V\text{-}s$, measured in the linear region with V_d=0.1 V.

2) Dual-gate 10-μm wide by 4-μm long transistors - these transistors are characterized at a drain voltage of 15 V as follows:

a) $I_{off\ (minimum)}$ - the minimum leakage current.

b) $V_g@I_{off(min)}$ - the gate voltage at which the leakage current ($I_{source\text{-}drain}$) is minimum, to indicate if the transistor is off at V_g=0 V; for pMOS transistors in the display, the value should be negative.

c) I_{on} - the drive current at a particular on-state condition.

d) V_t - the threshold voltage measured with V_d=0.1 V, done before the drain voltage is raised to 15 V to minimize any measurement induced effects.

e) V_{bd} - the drain breakdown voltage, which is defined as the drain voltage at which the source-drain current is 10 μA for zero gate bias.

f) Mobility - the maximum mobility of the transistor, in $cm^2/V\text{-}s$, measured in the linear region with V_d=0.1 V.

3) Single-gate 10-μm wide by 4-μm long transistors - probed at a drain voltage of 5 V for:

a) $I_{off\ (minimum)}$ - the minimum leakage current.

b) $V_g@I_{off(min)}$ - the gate voltage at which the leakage current ($I_{source\text{-}drain}$) is minimum, to indicate if the transistor is off at V_g=0 V; for pMOS transistors in the display, the value should be negative.

c) I_{on} - the drive current at a particular on-state condition.

d) V_t - the threshold voltage measured with V_d=0.1 V, done before the drain voltage is raised to 5 V to minimize any measurement induced effects.

e) V_{bd} - the drain breakdown voltage, which is defined as the drain voltage at which the source-drain current is 10 μA for zero gate bias.

f) Mobility - the maximum mobility of the transistor, in $cm^2/V\text{-}s$, measured in the linear region with V_d=0.1 V.

5.3 WAT Test Table

Table 5-1 illustrates the range of acceptable values for the various parameters described above. Three parameter value sets are provided. The first set, NOMINAL, defines typical values that are desirable for the production technology. The second set, WORST CASE, defines worst case values for production. The third set, STARTING, defines values that will be accepted at start-up in a foundry, but will probably have to be tightened to achieve optimum performance of the displays.

5.4 TFT Parameters

Parameters from three types of transistors, pixel, single-gate, and double-gate, were obtained from fully processed plates. Pixel transistors include lightly doped source and drain regions (LDD) and are 2.5 μm wide by 4 μm long. The other two transistors are 10 μm wide with a 4 μm gate dimension, without LDDs. The double-gate device is characterized as if the gate length were 8 μm. Testing bias conditions were selected to be appropriate to how the transistors operate in the circuit.

Probability plots—a typical approach taken in integrated circuit manufacturing—of the measurements were generated for the purpose of analysis. To illustrate the results, Figures 5-1 through 5-4 provide probability plots for some key parameters of pixel transistors and Figures 5-5 through 5-8 show some plots for single-gate devices.

Demonstrated, for example, is the achievement of leakage current in pixel transistors less than 1 pA for the entire distribution, with one-half of the population having leakage current less than 0.23 pA, the worst case value of Table 5-1. In the case of drive current, three pixel transistors in the population do not meet the worst case value. Threshold voltage is within the range defined by Table 5-1. For drain breakdown voltage, three transistors of the population have a value just under the 35-V worst case value. For the single-gate transistors, all fall within the allowed range for minimum leakage current and mobility. There are two exceptions to the allowed range for threshold voltage and one for drive current. Parameter distributions of this type are not unexpected during the prototype stage of development of a new technology.

Table 5-1. Summary of WAT measurements for pixel test chip.

		NOMINAL	WORST CASE	STARTING	UNITS
RESISTORS					
	P+ ACTIVE	400	<600	<600	Ω/square
	N+ GATE	2	<4	<4	Ω/square
	P+ CAPACITOR	200	<600	<600	Ω/square
	ITO	—	<1000	<1000	Ω/square
	P LDD	30K	<100K	<150K	Ω/square
CONTACT RESISTANCE					
	METAL TO P+ ACTIVE	—	<200	<200	Ω
	METAL TO N+ GATE	—	<15	<15	Ω
	ITO TO METAL	—	<500	<1K	Ω
TRANSISTORS					
PIXEL (at Vd = 10 V)					
	Ioff (min)	—	<.25	<5	pA
	Ioff (Vg=0)	—	<.25	<7.5	pA
	Ion	65	>25	>25	µA
	Vt	4.5	-2 to -6	-1 to -6	V
	Vbd (10 µA)	—	>35	>35	V
	Mobility	—	>20	>20	cm2/V-s
DUAL 4x10 (at Vd = 15 V)					
	Ioff (min)	—	<500	<1000	pA
	Vg@Ioff(min)	<0	<0	<0	V
	Ion	270	>105	>105	µA
	Vt	-4.5	-2 to -6	-1 to -6	V
	Vbd	—	>30	>30	V
	Mobility	80	40 to 120	40 to 120	cm2/V-s
SINGLE 4x10 (at Vd = 5 V)					
	Ioff (min)	—	<10	<10	pA
	Vg@Ioff(min)	<0	<0	<0	V
	Ion	450	>220	>220	µA
	Vt	-4.5	-2 to -6	-1 to -6	V
	Vbd	—	>15	>15	V
	Mobility	80	40 to 120	40 to 120	cm2/V-s

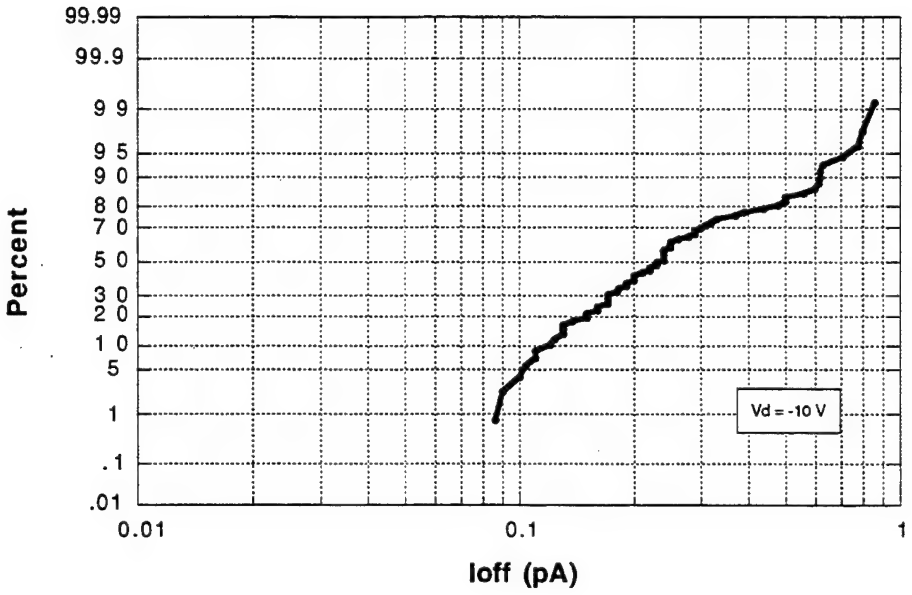


Figure 5-1. Probability distribution from pixel transistors at 10-V drain bias illustrating achievement of minimum leakage current less than 1 pA.

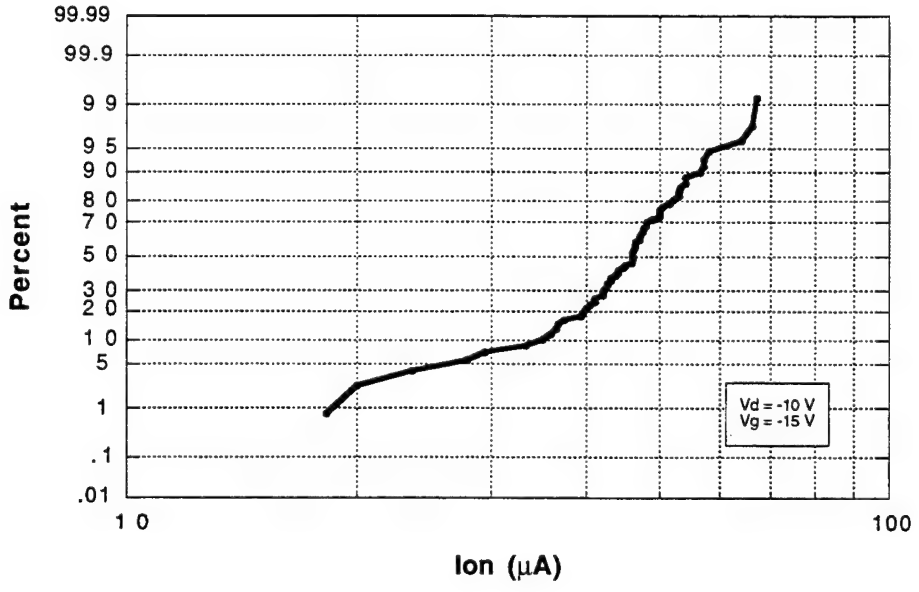


Figure 5-2. Probability distribution from pixel transistors illustrating drive current capability.

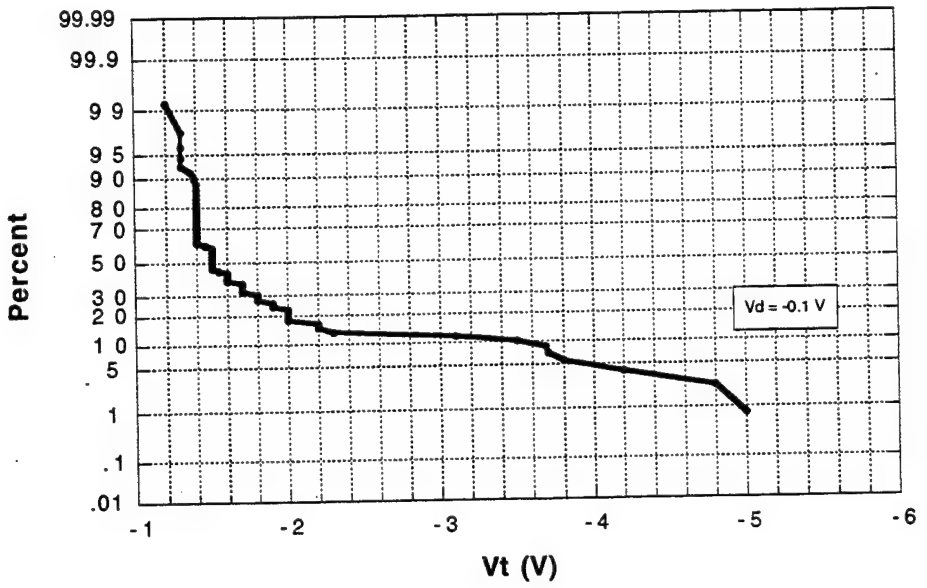


Figure 5-3. Probability distribution for threshold voltage from pixel transistors.

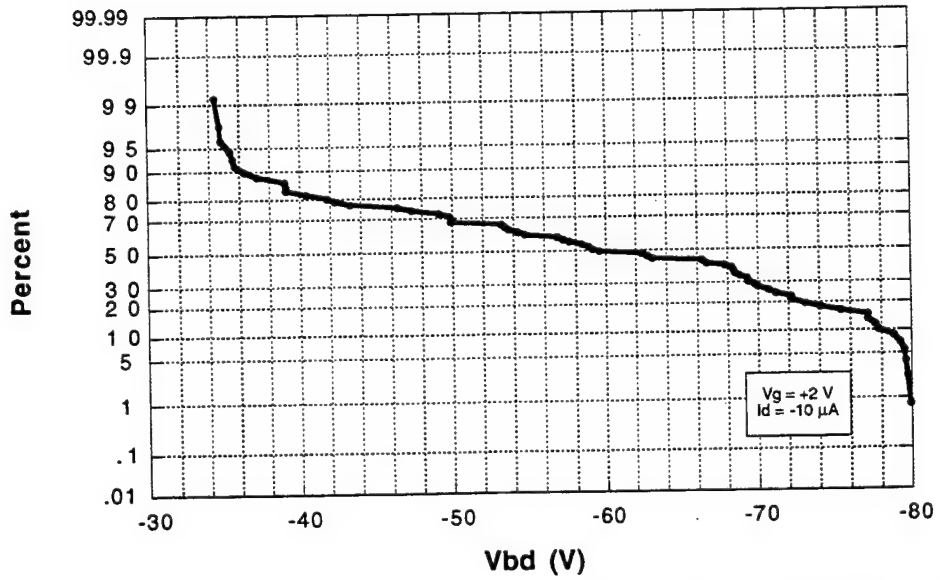


Figure 5-4. Probability distribution for drain breakdown voltage from pixel transistors illustrating large margin for device operation.

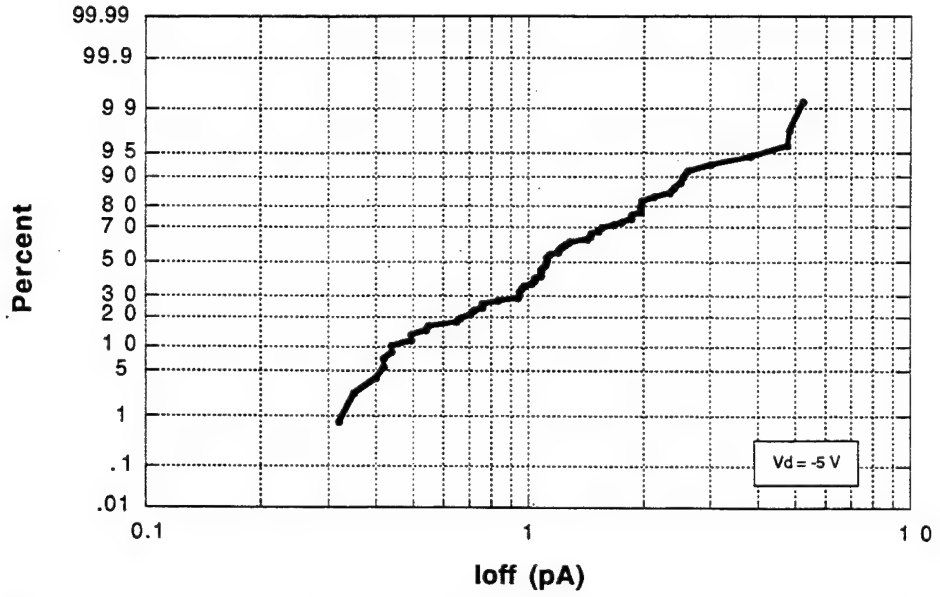


Figure 5-5. Probability distribution for minimum leakage current in W/L= 10µm/4µm transistors at 5-V drain bias.

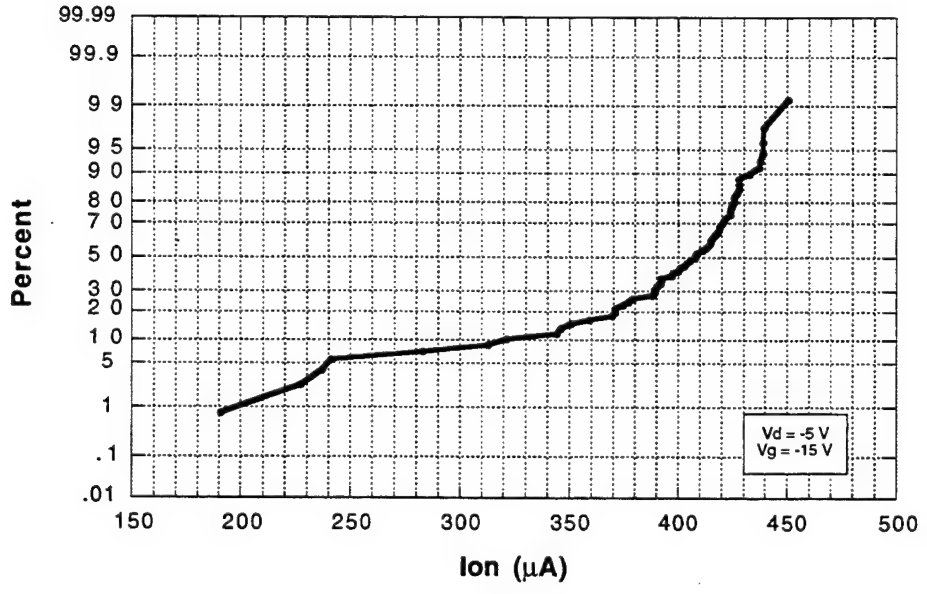


Figure 5-6. Probability distribution for drive current in W/L= 10µm/4µm transistors.

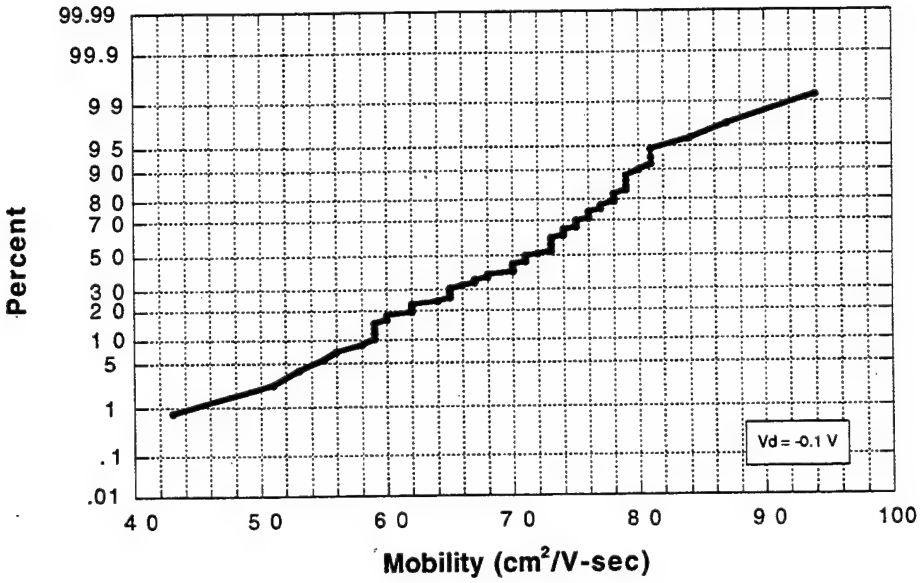


Figure 5-7. Probability distribution for mobility in W/L= 10μm/4μm transistors.

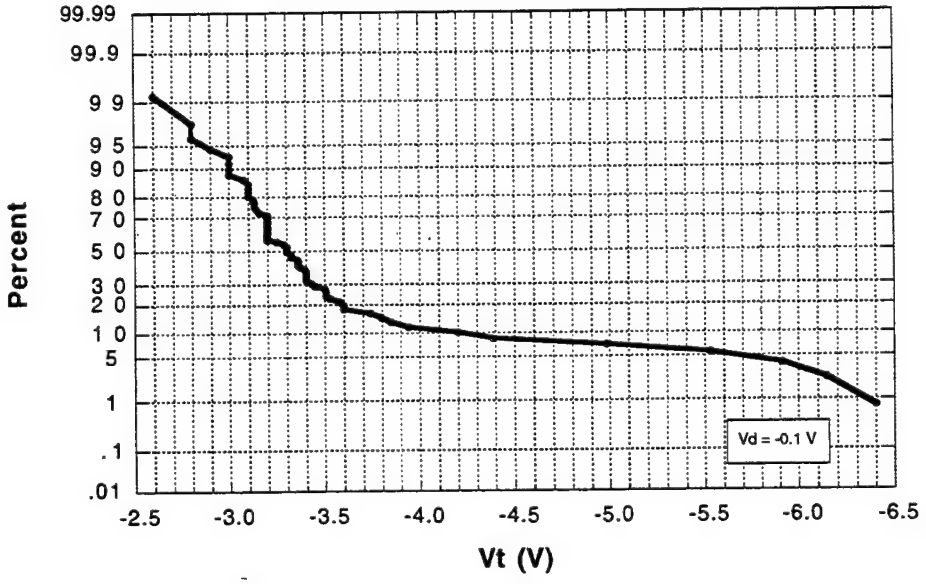


Figure 5-8. Probability distribution for threshold voltage in W/L= 10μm/4μm transistors.

6.0 1280 X 1024 DESIGN AND SPECIFICATION

6.1 Introduction

A detailed description of the display designed during the program is provided in the following sections. The operation of all key subcircuits is described, including the design-for-test features useful for wafer-level evaluation and repair. The detailed set of specifications, including electrical characteristics, timing diagrams, optical characteristics, suggested operating procedures, and pin assignments, is provided in the Appendix.

6.2 1280 X 1024 Design

The block and transistor level operation of the 1280 x 1024 polysilicon light valve (SRI020994) is described below. The valve incorporates a 37-µm x 37-µm monochrome pixel, producing a 6.1-cm (2.4-in.) diagonal viewable area. Pixel aperture exceeds 50% and display total luminous transmission is about 16%. Full field contrast ratio is in excess of 60:1 under optimum illumination conditions. The outer dimensions of the rectangular display are 53.9 mm x 47.5 mm.

Figure 6-1 provides a functional block diagram of the system. Data enters the display from a 16-channel analog bus connected to the input MULTIPLEXER. The multiplexer distributes data to a SAMPLE/HOLD block that is capable of acquiring and storing the 1280 values necessary to write one row of the display. After a row's worth of data is accumulated, it is passed to the DATA DRIVER, which frees the multiplexer and sample/hold for further input. The data driver forces an appropriate voltage onto each display column. Signal amplification and level shifting are accomplished in the data driver under control of signals RAMP, DATARAMP1, and DATARAMP2. Timing for the operations just described is provided by the TIMING block, which also controls vertical scanning of the display through signals supplied to the SELECT scanner. Four supplies provide system power and an externally applied potential, VCOMMON, sets the pixel common plane voltage.

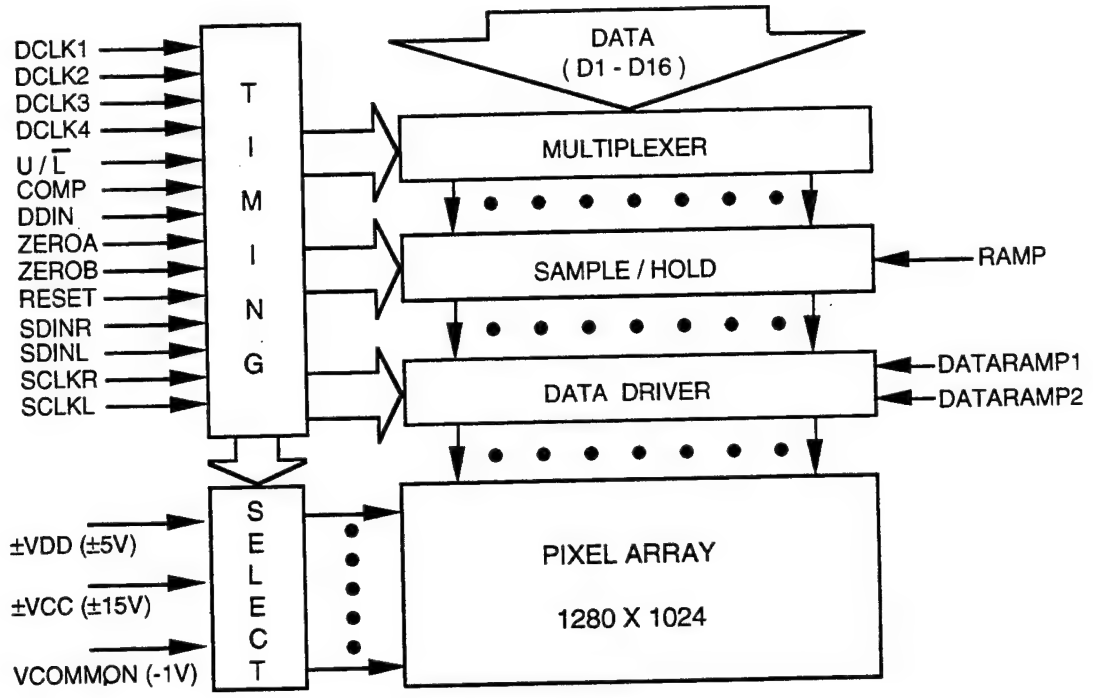


Figure 6-1. Functional block diagram of the 1280 x 1024 design.

The display accepts analog data in the range from 0 to 5 V with the low signal forcing minimum transmission of light and the high signal allowing maximum transmission. Data amplification and level shifting are provided on the display to produce a waveform suitable to drive the liquid crystal array. Timing block inputs, with the exception of DCLK1-DCLK4, are 5-V digital signals making the display easy to use. DCLK1-DCLK4 are 20-V clocks that synchronize data transmission. RAMP, DATARAMP1, and DATARAMP2 are nominally linear ramps controlling the amplification and level shifting of analog data. RAMP spans the range from -0.5 V to +5.5 V. DATARAMP1 and DATARAMP2 have endpoints of -1 ± 6 V.

6.2.1 Multiplexer and Sample/Hold

High resolution displays require wide bandwidth data channels. The bandwidth per channel can be minimized by continuous transmission on each channel. A key feature of the multiplexer and sample/hold circuits employed in the 1280 x 1024 polysilicon light valve is that they approach

the minimum required bandwidth per channel without the need for excessively large transistors and without serious corruption of the data from switch feedthrough.

Figure 6-2 details the multiplexer and sample/hold functions that are merged at the transistor level, although they are shown as distinct entities in the block diagram of Figure 6-1. These functions are implemented in such a way that the bandwidth minimization mentioned previously is achieved. Sixteen analog input channels (D1-D16) are split into upper (D1U-D16U) and lower (D1L-D16L) data paths. Each column of the display is capable of receiving data from an upper path during the times that even display rows are written and from a lower path when odd rows are selected. Two capacitors for each display column serve to sample the analog data. One capacitor samples during odd row times and the other for even row times. Time-interleaving the capacitors in this way means that while one capacitor is sampling new analog data the other capacitor can output its previously stored information to the column. This affords the maximum time possible for the sampling process and for driving the column line.

In Figure 6-2, the two left-most capacitors which connect to D1U and D1L, belong to display column 1. Correspondingly, the rightmost capacitors service column 16, while column 17 (not shown) would have its capacitors attached again to D1U and D1L. Capacitors sample analog data when the capacitor bottom plate is switched to +VDD. Alternatively, sampled data is output to a column line by connecting a bottom plate to VCIN. Sampling analog data and outputting it to display columns is controlled by signals SR, SR´, S1P, and S1P´.

Consider the case when SU is low and SL is high. This corresponds to writing even numbered display rows. Analog data passes from input channels D1-D16 to the upper data bus D1U-D16U. The lower data bus is connected to the RAMP input. Columns 1-16 will sample analog data when S1P pulses low and similarly for columns 17-32 when S2P (not shown) is pulsed. Previously sampled data is output to all columns when SR´ is switched low. Note that S1P´, S2P´, and SR are not used for the case of SU low and SL high. They will be used when SU is high and SL is low, which corresponds to outputting data for odd rows.

6.2.2 Data Driver

The data driver receives data from the multiplexer and sample/hold block in the form of voltages stored on sampling capacitors allocated to the columns. The bottom plates of the chosen capacitors are connected to the data driver inputs under control of SR´ or SR. The capacitor top plates connect to the RAMP signal as determined by SU or SL. These details have been previously discussed and are illustrated in Figure 6-2. The input signals to the data driver are therefore seen to be the sum of the RAMP input and the sampled analog video.

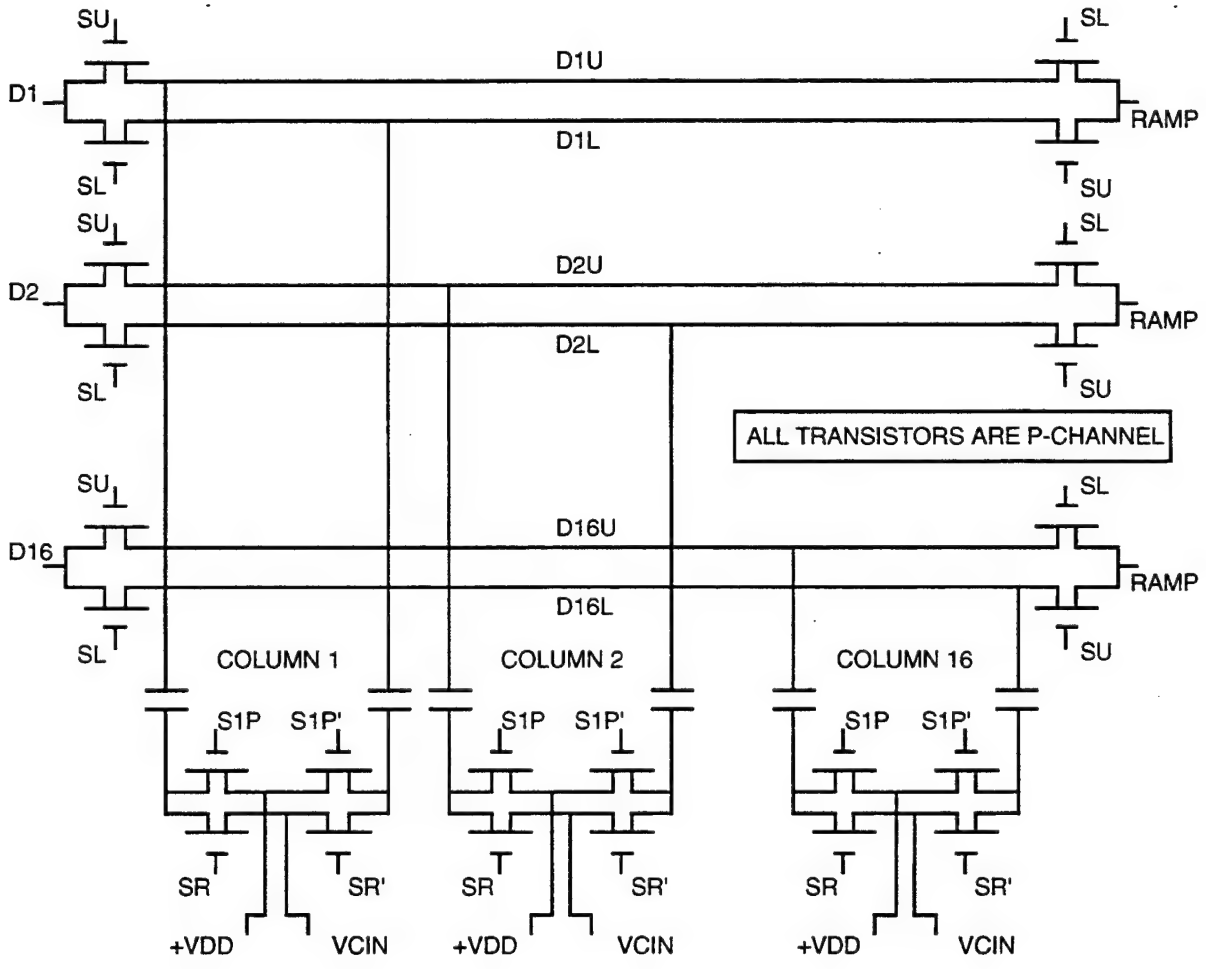


Figure 6-2. Multiplexer and sample/hold circuits.

Figure 6-3 provides further information pertinent to operation of the data driver. A comparator receives the voltage VCIN for a particular column and determines when VCIN is equal to +VDD. VCIN has the shape indicated in the figure and always begins to ramp at a voltage level above +VDD and ends at a level below +VDD. As VCIN is the sum of the RAMP input and the analog data, switching of the comparator occurs at a time that is data dependent. The comparator output is connected to the gate of transistor P4. Assuming P3 is on, P6 is off, and node 2 is initialized low, then the switching of the comparator output from high to low will disconnect the appropriate display column line from DATARAMPX when VCIN ramps low. Hence, the column line will store the DATARAMPX value occurring at the moment the connection is broken and deliver this voltage to the pixel array. In essence, the data driver circuit of Figure 6-3 performs an analog-to-analog conversion between video data and the voltage output to a pixel. The conversion is under the control of RAMP and DATARAMPX where DATARAMPX represents either DATARAMP1 or DATARAMP2. Suitable choices of the controlling waveforms can provide an analog to analog conversion exhibiting gain, signal inversion, and level shifting as required by the LCD pixel. Nonlinear conversions are also possible to provide for gamma correction.

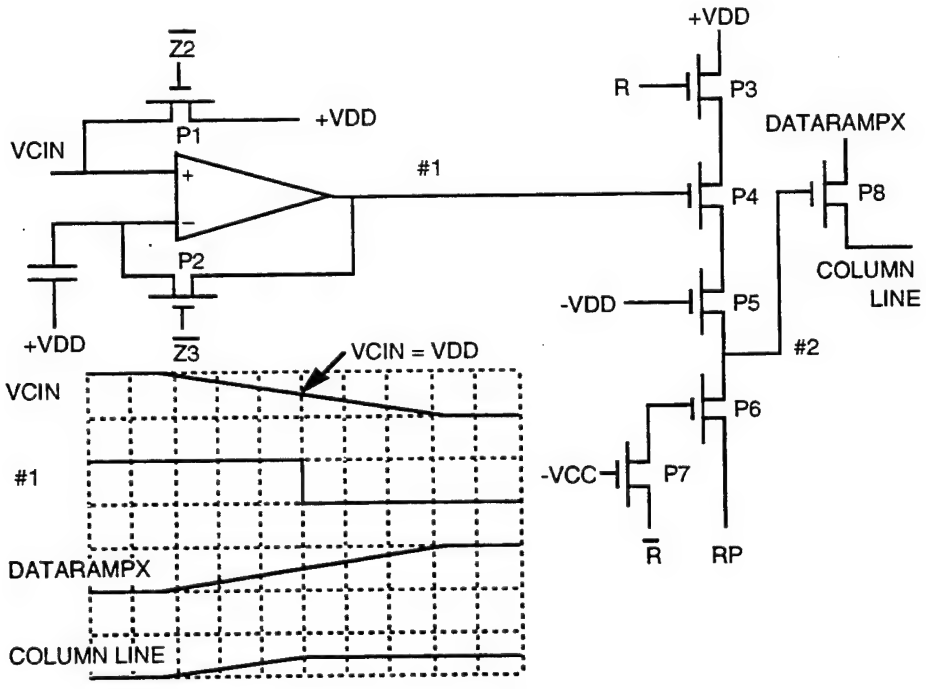


Figure 6-3. Data driver circuit.

6.2.3 Select Scanner

Vertical scanning of the pixel array is accomplished by the select scanner. A transistor level representation of four scanner stages is depicted in Figure 6-4, along with waveforms to illustrate scanner operation. A row of pixels is selected for receipt of data when the appropriate scanner output switches low and capture of data occurs on the rising edge of the driving waveform. As is seen in the figure, more than one row is selected at a time, because rows are preselected to compensate for the slow response of polysilicon lines crossing the pixel array. In this case, preselected means that a row is switched low prior to the arrival of data to be captured by that row. Referring to Figure 6-4, notice that row # 2 switches low during the time that data for row #1 is being delivered to the array and stays low until row # 2 data can be captured. Early selection of rows relaxes the requirement for low resistivity select lines.

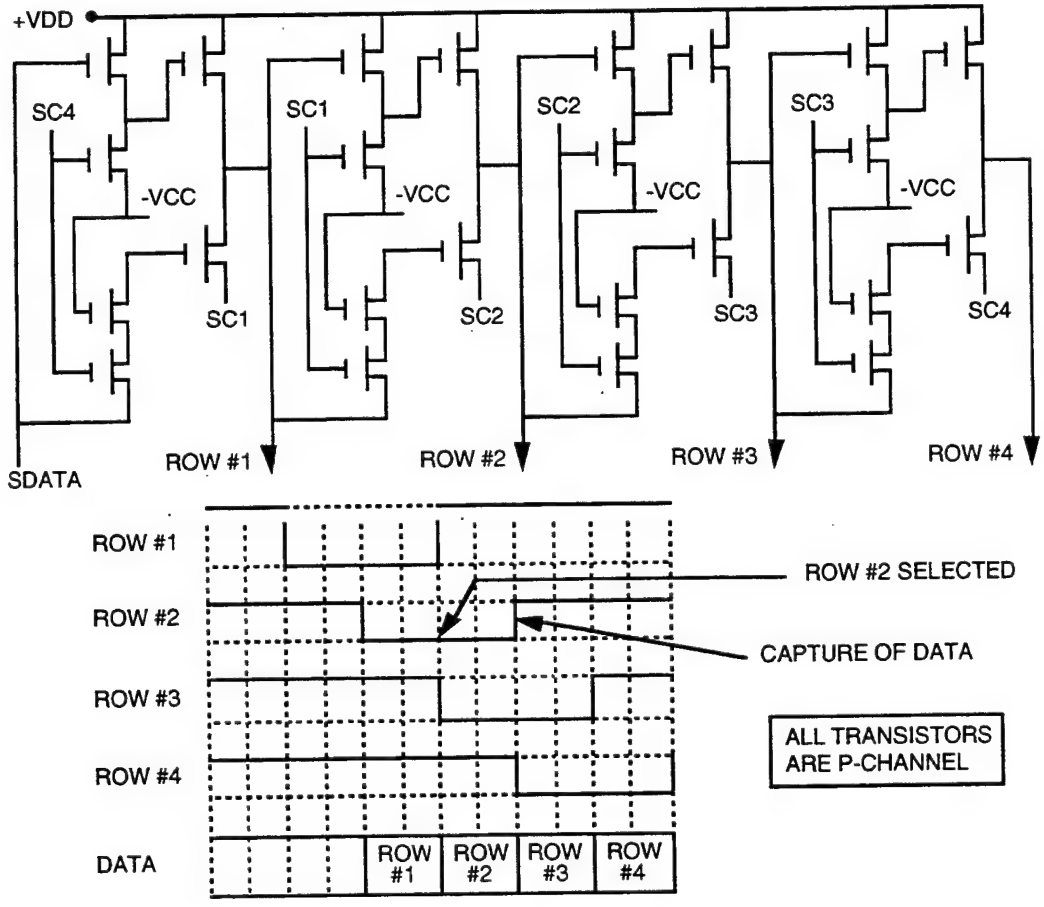


Figure 6-4. Select scanner circuit.

6.2.4 Timing

The timing block synthesizes all internal waveforms required to control the display. Inputs to the block are mapped into the necessary outputs to drive the multiplexer, sample/hold, data driver, and select scanner. Functions performed by the timing include amplification and level shifting of 5-V digital inputs plus logic operations for waveform synthesis.

SCLKR and SCLKL are the select scanner clocks that control the rate at which vertical scanning of the pixel array takes place. The array is scanned at the clock rate in response to a trigger provided by SDINL and SDINR. In Figure 6-4, the signals SC1 - SC4 and SDATA are created from SCLKR, SCLKL, SDINR, and SDINL. With reference to Figure 6-2 and the related discussion, DDIN and DCLK1 - DCLK4 synchronize data transmission to the display since S1P, S1P′, S2P, S2P′, ... are derived from these signals. U/$\overline{L}$, COMP, ZEROA, ZEROB, and RESET sequence events in the multiplexer, sample/hold, and data driver. Sequencing is effected by producing SU, SL, SR, SR′, $\overline{Z2}$, $\overline{Z3}$, R, $\overline{R}$, and RP from Boolean operations on these five inputs.

6.2.5 Pixel Array

The array is a conventional active matrix array incorporating a storage capacitor, an ITO control electrode, and a p-channel access transistor for each pixel. Capacitor formation and layout are optimized to produce a high capacitance pixel without sacrificing pixel aperture. The control electrode is used to effectively shield the liquid crystal fluid from stray electric fields that could induce undesirable effects in pixel performance.

6.2.6 Built-In Test Circuits

Test circuits are integrated into the SRI020994 to facilitate wafer level go/no-go electrical evaluation of the display and to enhance laser repair procedures. Six test pads, located at the edge of the display and merged with the normal signal pads, permit easy access to test circuit outputs. Figure 6.5 indicates how select scanner (vertical scanning) signals are multiplexed to two test pads.

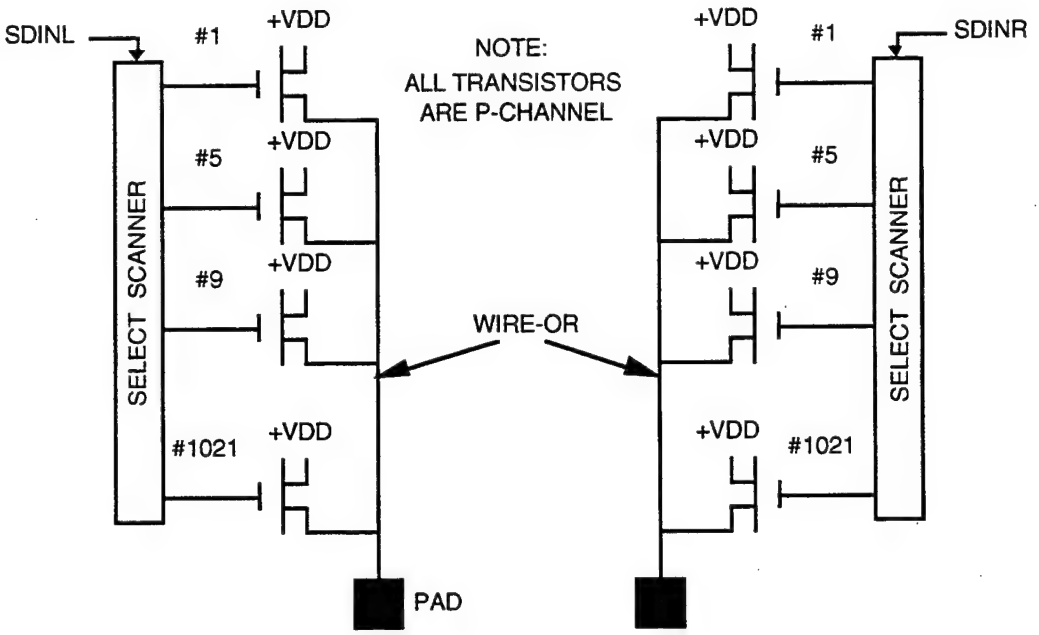


Figure 6-5. Left and right select scanner multiplexers.

A digital multiplexer is formed by wire-oring mutually exclusive scanner outputs and connecting the resultant signal to a single test pad. A separate multiplexer exists for each of the redundant right and left select scanners. Since the right and left scanners can be loaded independently via SDINL and SDINR, it is possible to observe scanner operation by looking at the waveform present on the appropriate test pad. Go/no-go testing is implemented by checking for the correct waveform. Interpretation of incorrect waveforms can yield necessary spatial information for effecting laser repairs.

Data scanner (horizontal scanning) signals are also multiplexed together, but in this instance four test outputs are produced. Figure 6-6 illustrates the data scanner multiplexers. The gate of a pMOS transistor is connected to each data line and again wire-oring is used to produce the desired test outputs. Every fourth data line is multiplexed into a common output pad. Waveform observation and interpretation provides go/no-go testing of the data scanners and information for laser repair if appropriate data is fed to the display.

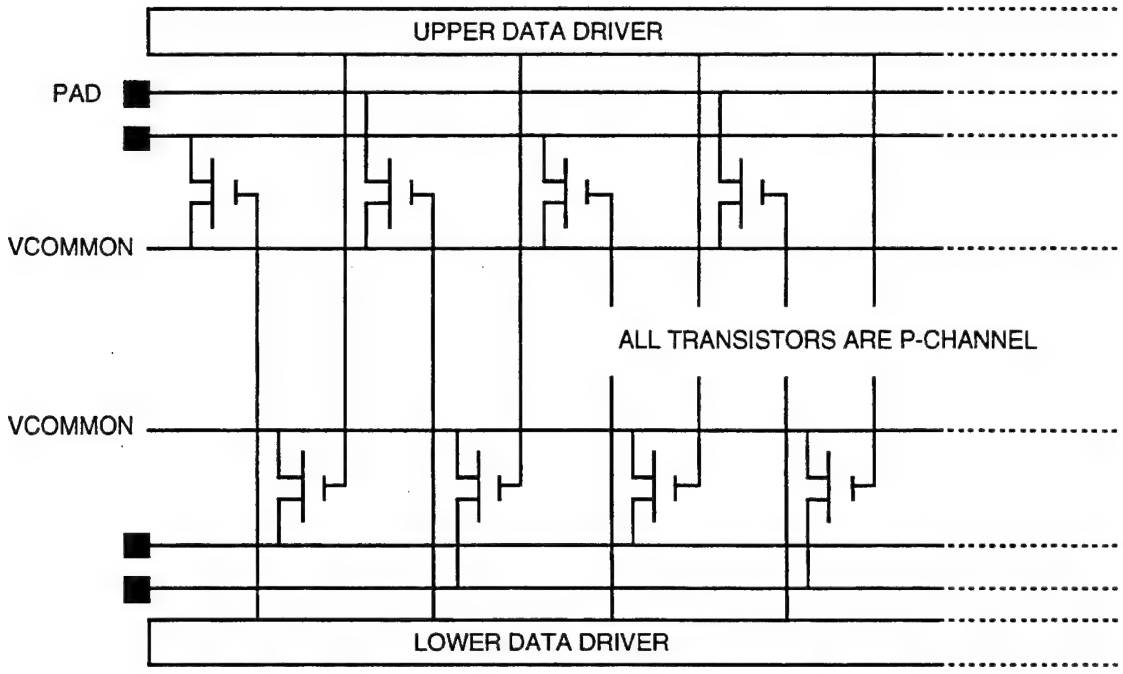


Figure 6-6. Upper and lower data scanner multiplexers.

6.2.7 Temperature Compensation

The data driver, as previously described, performs an analog to analog conversion, mapping analog video data into the appropriate drive voltage for a pixel. The conversion process exhibits some temperature sensitivity resulting primarily from the temperature dependent propagation delay of the data driver circuit. When required, it is possible to compensate for this behavior. Four extra data drivers are included on the display, one in each corner. These drivers share a common input, TC-IN, as indicated in Figure 6-7.

TC-IN is sampled and held before it is applied to the extra data driver blocks. Each driver receives as an input the sampled TC-IN value, summed with the same RAMP input that is fed to all other data drivers in the display. This means that TC-IN is processed by the extra drivers just as video data is processed by the normal drivers. For example, the top left driver disconnects its output from DATARAMP2 when RAMP summed with the sampled value of TC-IN causes the input to the driver to equal +VDD. The driver output takes on the specific DATARAMP2 value

present at the time of disconnection assuming some holding capacitance is present at the output of the top left driver.

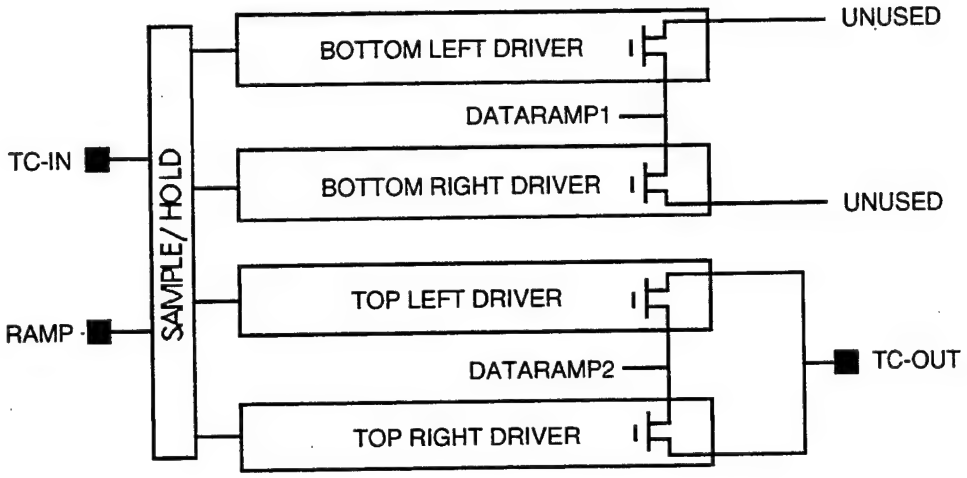


Figure 6-7. Temperature compensation circuit

In the present design, the top left and top right drivers are combined at an output pad TC-OUT, possible because both drivers operate from DATARAMP2. TC-OUT holds the DATARAMP2 value output by the slower of the two drivers. The bottom left and bottom right drivers are not brought out to a pad but are included for possible refinements of the temperature compensation circuitry.

Ideally, a fixed value of TC-IN would produce a fixed value of TC-OUT. If TC-OUT is observed to change it is the result of changing driver behavior, most probably propagation delay. Appropriate adjustment of the RAMP rate of change, achieved by modifying the voltage end points, can stabilize TC-OUT. The adjustment is easily accomplished with off-display circuitry to create a feedback loop. The loop also guards against driver behavioral changes that may be induced by sources other than temperature, for example power supply drift. Stabilizing TC-OUT causes all drivers in the display to be stabilized, if all drivers share a common environment and are reasonably well matched.

6.3 1280 X 1024 Specification

In the Appendix, a complete description and preliminary specifications for the 1280 x 1024 display are provided. Included are electrical characteristics, timing diagrams, optical characteristics, suggested operating procedures, and pin assignments.

7.0 DISPLAY TEST

7.1 Introduction

This section highlights key aspects of the approach taken for test and evaluation of the 1280 x 1024 polysilicon light valves. The overall test strategy was divided into electrical and optical test programs. Emphasis is given to the electrical test work, as it constituted the major part of the effort. Described in the following section are the test strategies developed, the test programs defined, repair and rework approaches developed, and test results achieved. A later section summarizes the optical test work.

7.2 Electrical Testing

A strategy for electrical evaluation of the light valve design was developed to permit key information to be obtained as early as possible during the flow of display plates through the fabrication process. This general approach to testing permits early detection of any design errors and enables problems to be identified at major steps in the flow of plates from TFT wafer processing through final assembly. To execute the test strategy, electrical test programs were defined to perform tests at specific times in the fabrication cycle:

1. Circuit block after metallization — to verify operation of all major circuits;
2. Active matrix plates — to verify bus design and processing success, by probing for input shorts and select and data scanner operation; and
3. Assembled display — to verify correct assembly, top plate processing, and light valve operation to specification.

Testing of the active matrix plate can be done at two different times in the fabrication sequence: just after metallization to form the TFTs and after complete processing into assembled displays. In the former case, it is possible to do repairs of most types of defects; in the latter case,

rework is very limited because of the various additional layers that are present on the finished device structure.

Division of the test programs into these categories allows for successive testing of each light valve throughout wafer processing and display assembly, and can be used to track processing problems through each step of a manufacturing sequence. In a manufacturing environment, the test programs would be more in the nature of GO/NO-GO; whereas for our purposes here, information useful for failure analysis and design verification was of primary interest.

7.2.1 Circuit Blocks after Metallization

7.2.1.1 Test Procedures

All of the logic and circuit building blocks in the 1280 x 1024 design are incorporated into circuit test structures. Everything from primitive logic building blocks such as inverters and nand gates up to complex circuit blocks, pictured in Figure 6-1, including timing, multiplexer, sample/hold, select scanners, and data drivers are available. To accommodate all of the circuit blocks that are part of the display design requires four test circuit arrays each with 48 pads. The test arrays are repeated at six locations on the wafer, three above the 1280 x 1024 display and three below it; Figure 7-1 illustrates the layout of a wafer with one of the four test circuit arrays indicated.

The circuit blocks were tested with a manual probe station, shown schematically in Figure 7-2. The motherboard in the set-up is the same as that of the portable testbed, which is used for optical testing and evaluation of assembled displays. The motherboard generates the required analog signals including the data and reference ramps. A daughterboard is appended onto the motherboard for evaluation of the circuit test structures; the daughterboard level-shifts the 5-V digital signals to the appropriate voltage range required by the circuit blocks. The HP signal generator produces the 5-V digital logic signals for the particular circuit under test. Individual cables between the probe card and the motherboard multiplex logic signals to the circuit under test for each of the four test arrays.

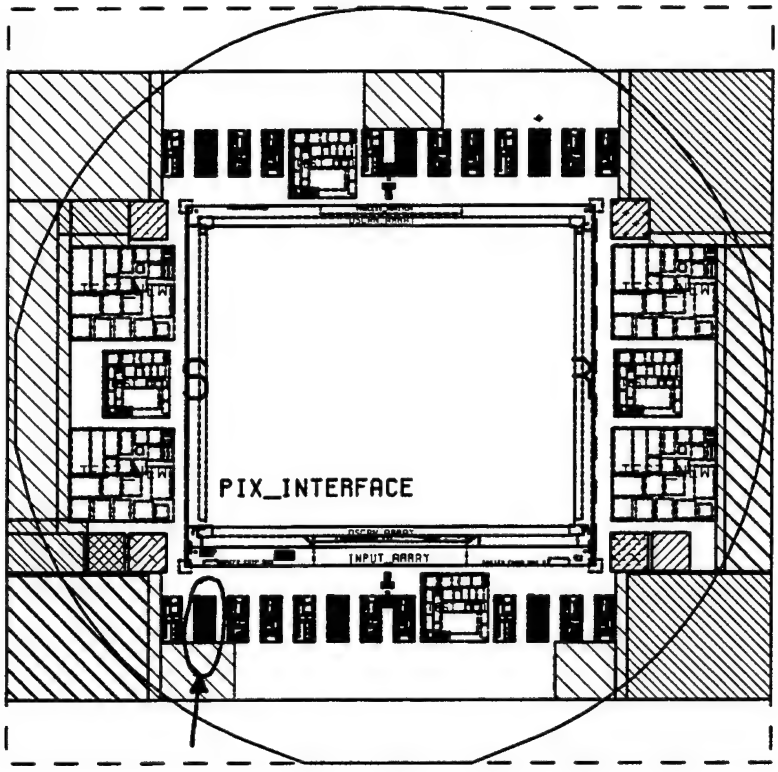


Figure 7-1. Layout of 1280 x 1024 display wafer with a circuit array indicated.

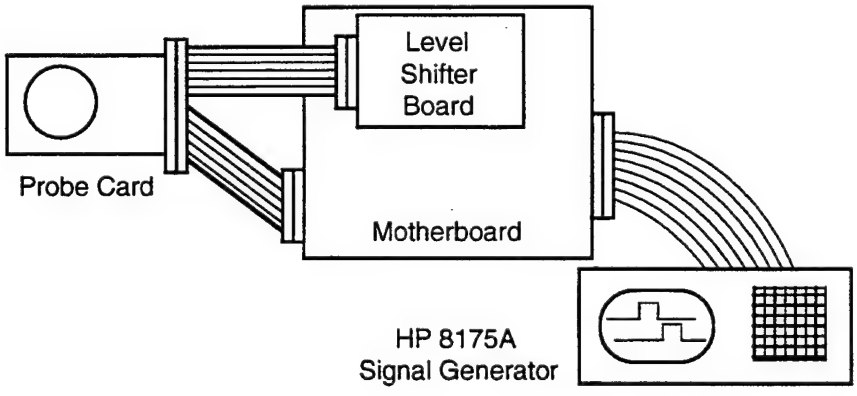


Figure 7-2. Schematic of test set up for manual probing of circuit test structures.

7.2.1.2 Test Results

Manual testing of the circuit blocks focused on determining if any deficiencies in the design existed such that the display would not perform to specifications. Consequently, the circuits under test were not fully characterized for failure conditions. It was determined, for example, that the select scanner was completely functional and operated to specified voltage and frequency, but the frequency at which the select scanner failed was not within the scope of work.

Manual testing verified that all of the logic and analog circuit blocks used in the display operate to specifications. A representative sample of results, including waveforms for inverter, nand, and data driver multiplexing signals, are shown in Figures 7-3a through 7-3f. These results can be compared with the specifications included in the Appendix to confirm that the circuit operation conforms to the specifications.

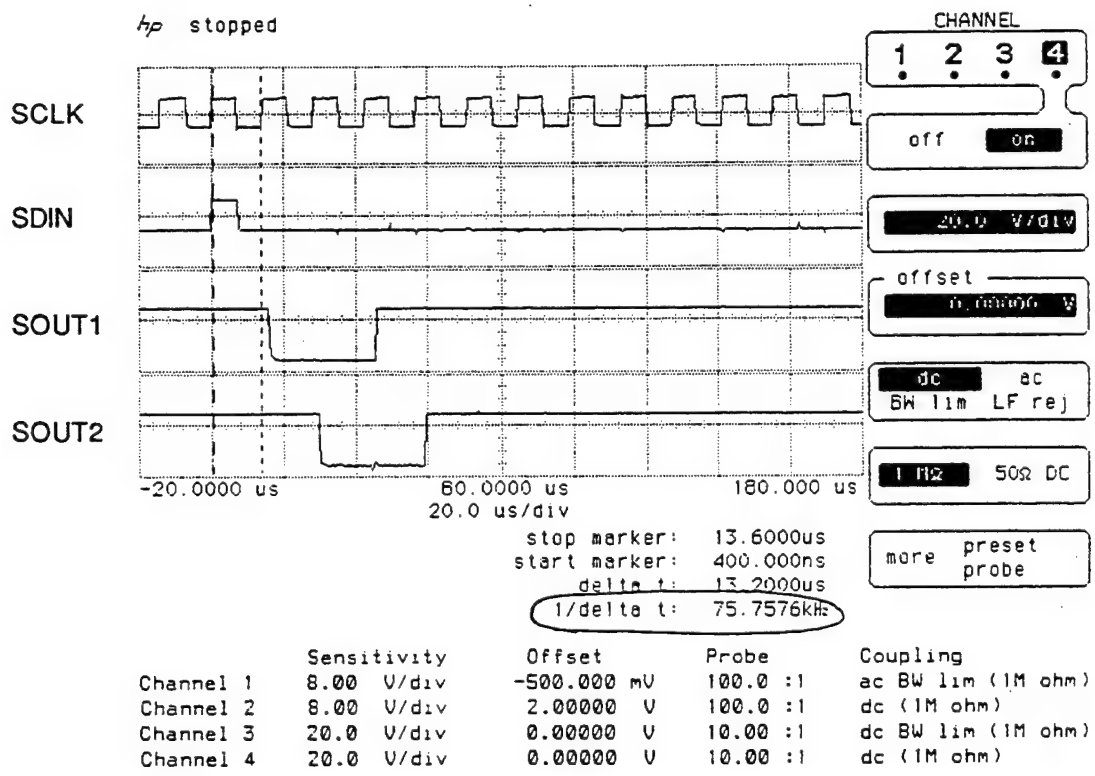


Figure 7-3a. Output of first and second select scanner stage referenced with the control signals SCLK and SDIN.

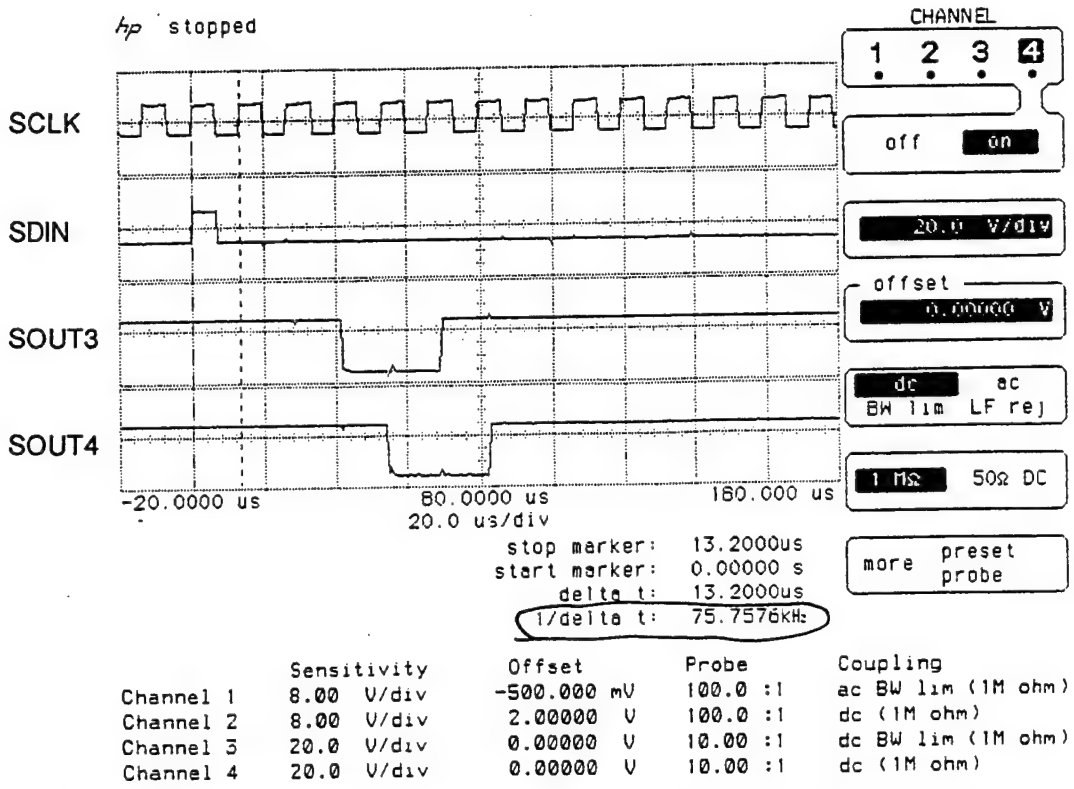


Figure 7-3b. Output of third and fourth select scanner stage referenced with the control signals SCLK and SDIN.

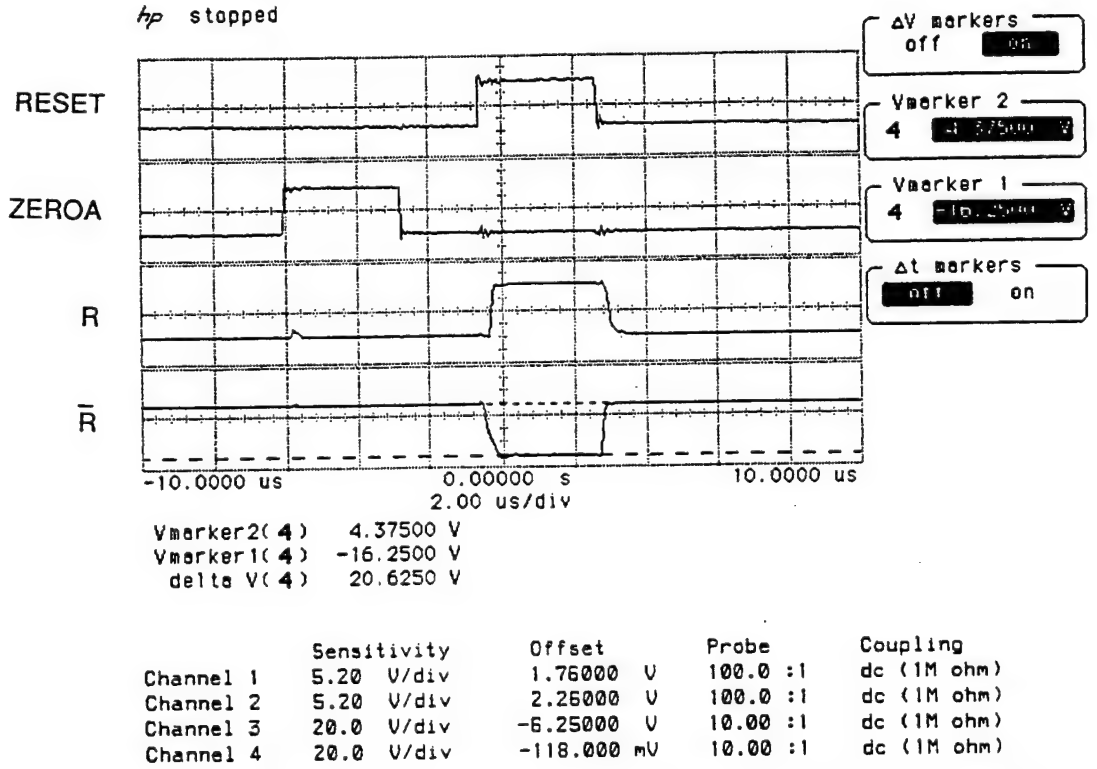
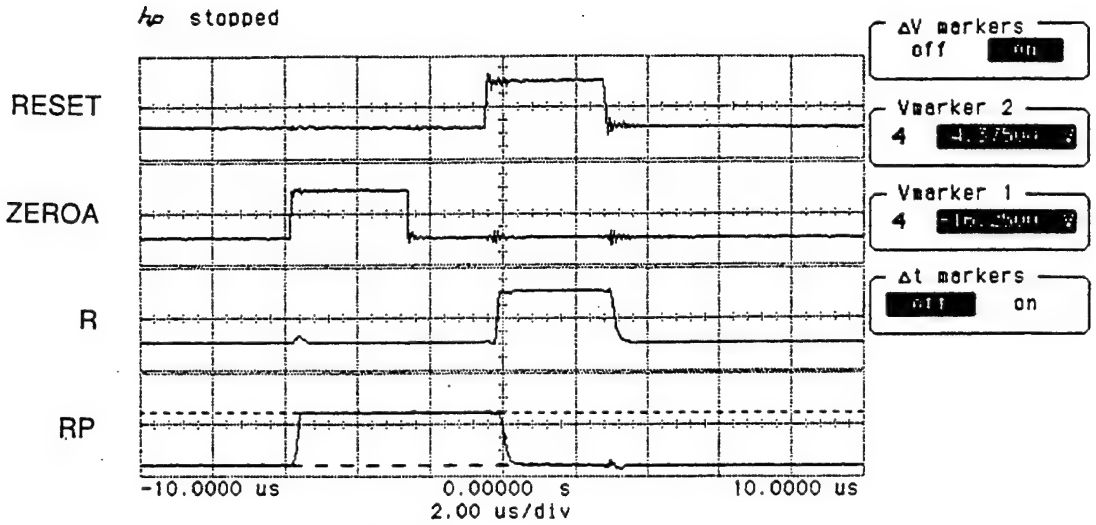
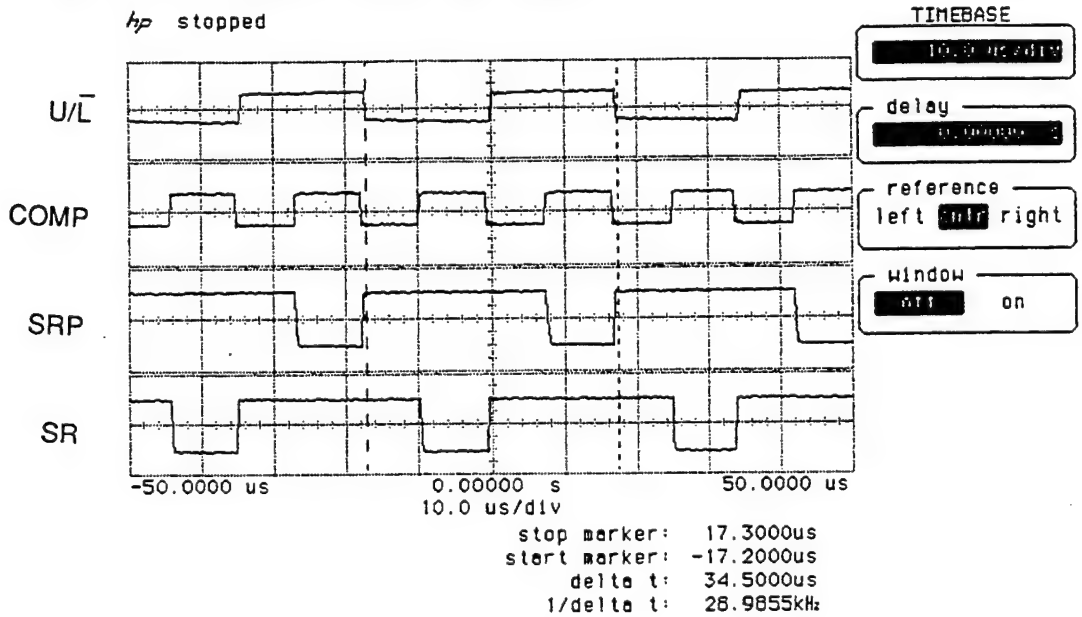


Figure 7-3c. Output of internally generated signals R and $\bar{R}$ referenced with the control signals RESET and ZEROA.



	Sensitivity	Offset	Probe	Coupling
Channel 1	5.20 V/div	1.76000 V	100.0 :1	dc (1M ohm)
Channel 2	5.20 V/div	2.26000 V	100.0 :1	dc (1M ohm)
Channel 3	20.0 V/div	-6.25000 V	10.00 :1	dc (1M ohm)
Channel 4	20.0 V/div	-118.000 mV	10.00 :1	dc (1M ohm)

Figure 7-3d. Output of internally generated signals R and RP referenced with the control signals RESET and ZEROA.



	Sensitivity	Offset	Probe	Coupling
Channel 1	8.00 V/div	1.75000 V	100.0 :1	dc (1M ohm)
Channel 2	8.00 V/div	1.75000 V	100.0 :1	dc (1M ohm)
Channel 3	20.0 V/div	4.37500 V	10.00 :1	dc (1M ohm)
Channel 4	20.0 V/div	5.00000 V	10.00 :1	dc (1M ohm)

Figure 7-3e. Output of internally generated signals SRP and SR referenced with the control signals U/$\bar{L}$ and COMP.

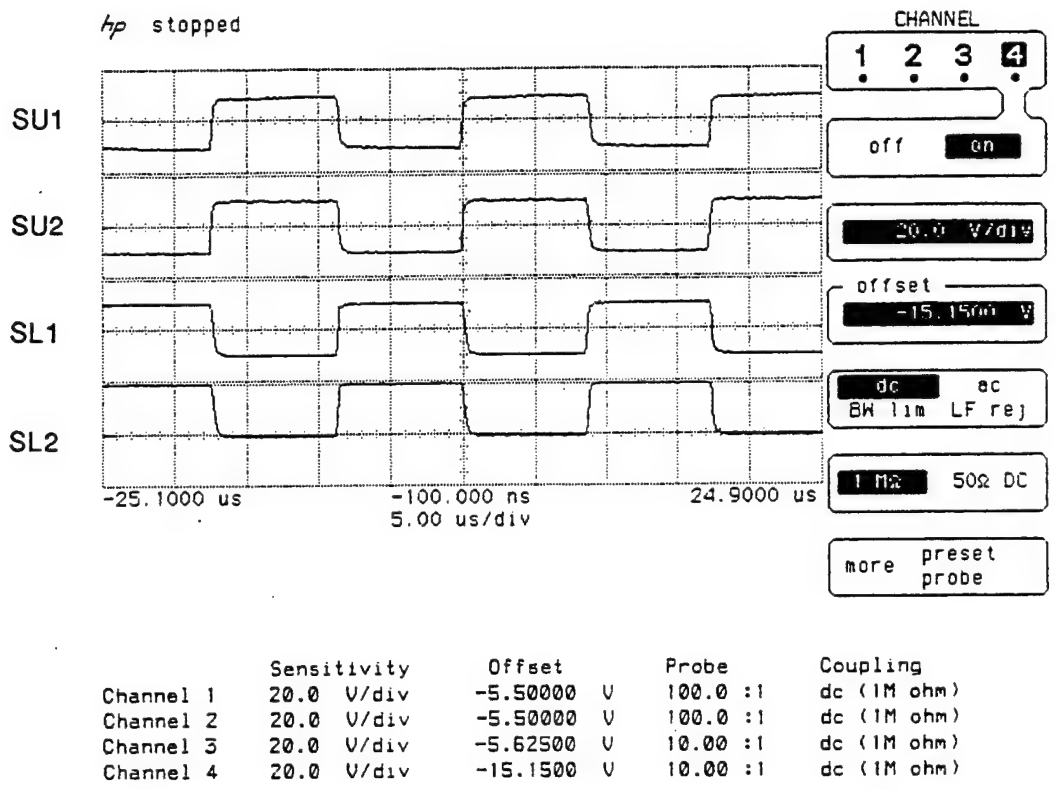


Figure 7-3f. Output of SU1, SU2, SL1, and SL2 generated from U/$\overline{L}$ (not shown).

7.2.2 Active Matrix Plates

7.2.2.1 Test Flow and Equipment

Figure 7-4 summarizes the test flow used for electrical evaluation of active matrix plates before and after metallization. Primarily a research tool to analyze the process, the fabricated devices, and the functionality of the completed 1280 x 1024 active matrix plates, this test sequence is not suitable for a manufacturing environment. For manufacturing, a test sequence would involve a simple GO/NO-GO test of the select and data scanners, examination of select and data line opens, and determination of select-to-data shorts. The design of the 1280 x 1024 display does support such a test sequence appropriate for manufacturing.

The test sequence described in this section is intended not only to determine if the array is functioning according to the design specifications, but is also used for rework of faulty displays and for failure analysis. Each step in the testing sequence and how it is executed are described in detail below.

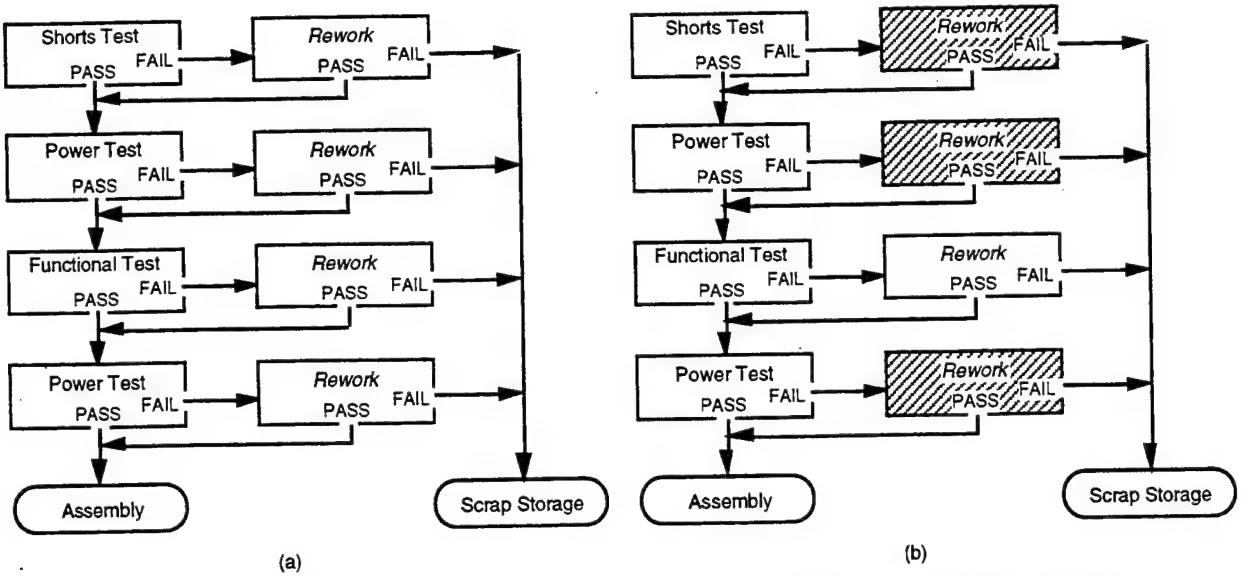


Figure 7-4. Test flow for active matrix plates: (a) after metallization and (b) after complete processing. In shaded areas plate rework is severely limited.

Figure 7-5 illustrates the test equipment used for test and repair of active matrix plates. The heart of the system is an HP217 computer, which controls the test equipment through an IEEE-488 bus. An HP8175A generates all of the switching signals from 0-5V that are appropriately level-shifted for the active matrix plate. The display plate is affixed to a DCI12X12P test bed, which can be independently translated in two directions under control of the HP217 computer. All of the waveforms are captured by an HP54501A digital oscilloscope. Plate reworking is accomplished on the same station with a Florod LCM laser repair system, which allows voltages and currents to be monitored simultaneously with laser repair.

7.2.2.2 Test Procedures after Metallization

Subsequent to wafer acceptance test and before powering up a display, the test flow of Figure 7-4 was followed. A Shorts Test on the input leads was first executed. If shorts were present, the array was examined to determine the cause of the shorts. The examination consisted of manually probing the shorted pins and measuring the resistance between the probes while the probes were traced through the display. Once the source of a short was found by this technique, it

was removed by laser cutting. This procedure was repeated until all input shorts were removed from the active matrix plate under test.

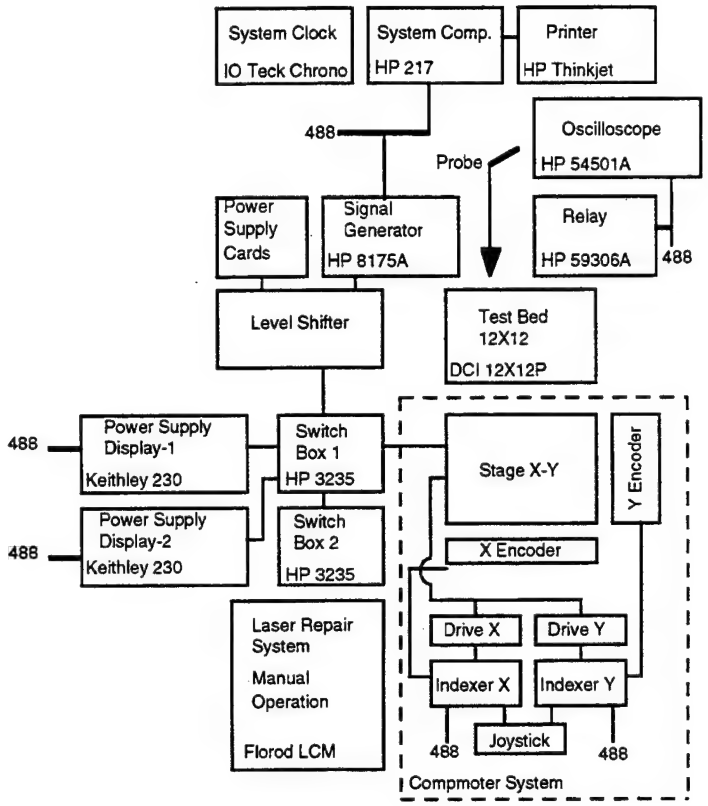


Figure 7-5. Equipment diagram for shorts and functional testing.

Once the input leads were cleared of all shorts, a Power Test was done by application of bias to the plate and measurement of the current drawn from the power supplies. If the current drawn exceeded the design specification, the plate was again examined for internal shorts associated with the power busses. All shorts to the power busses must be cleared before the array can be functionally tested.

After the active matrix plate passed the Power Test, the Functional Test routine was exercised by application of the clock and data signals to the full plate; the signals applied were identical to those used in normal display operation with the exception that a lower frequency was used. At the end of each select/data scanner is a pad that can be used to monitor the signal seen by the select/data

line. Under functional test, these pads were manually probed to determine if each data and select scanner circuit was operating properly. Since each select scanner stage is dependent on operation of the previous stage, testing the correct operation of select scanners is accomplished by confirming the presence of a select pulse at the output of the last stage. If a select pulse is present, the previous select scanners, most likely, are all operational. At present, a similar technique is not possible with the data scanners; each data scanner must be tested separately.

If certain select scanners did not pass the functional test, the display was reworked through laser repair. The display is designed with redundant select scanners, important because a failure in a select scanner stage results in the failure of all subsequent select scanner stages. Each select line is driven by a pair of select scanners, one each on the left and right side of the display. Laser repair sites are built into each select scanner stage to permit removal of the stage from its bank, left or right. Thus, if a select scanner is functioning incorrectly, the non-functioning stage is removed from its bank by laser cutting. Then, the select scanner stage following the non-functioning stage will be driven by the functioning select scanner stage from the opposite bank. Figure 7-6 represents the case of the left select scanner stage (n+1) not functional. Laser repair removes the left select scanner stage by opening a line. The left select scanner stage (n+2) now receives a pulse from the right select scanner stage (n+1), thus maintaining operation.

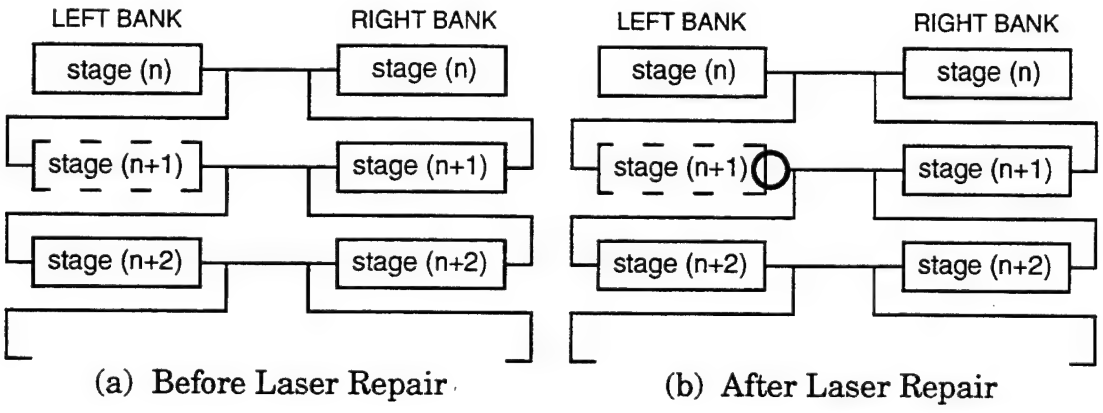


Figure 7-6. Select scanner redundancy allows laser repair to remove a non-functioning select scanner and maintain operation from the opposite bank.

If any data scanners did not pass functional testing, the display was again reworked through laser repair. Unlike the select scanners, the data scanners have no built-in redundancy. The only repair currently possible is nearest-neighbor shorting, which allows the same data to be applied to two adjacent data lines, thus eliminating any open or partially open lines. Generally, these time consuming repairs were only used to make demonstration displays. In high volume manufacturing, displays would be discarded if the data scanners were not fully functional or if any data lines were found to be open.

If all of the select and data scanners passed functional testing, the displays had to pass a final Power Test before shipment for assembly. This power test determines if any of the rework procedures introduced power line shorts.

7.2.2.3 Test Procedures After Complete Processing

Fully processed active matrix plates were tested with the same test sequence as that used after metallization. However, rework of fully processed plates is more difficult than rework of plates just after metallization. Plates that fail Shorts and Power tests cannot be successfully reworked without a significant time penalty.

Shorts reworking is more difficult to do since fully processed plates have an overcoat, which prevents circuit probing within the array. Thus, shorts cannot be found by the internal probing technique discussed earlier. Shorts can be found by optical inspection, and once found, can still be cleared by laser cutting. However this process is now performed with greater difficulty than before, resulting in an added time penalty.

Test-and-repair of select and data scanners is not affected by the presence of the overcoat since the test pads and laser repair sites are all available. Hence, this procedure is identical to that described in section 7.2.2.2.

7.2.2.4 Test Results

During the early phase of a new design effort, it is expected that less than 100% functionality would be typical. On these early active matrix plates, input shorts were cleared, i.e. reworked,

with great success; however, clearing of input shorts is a time-consuming process. Consequently, reworking for shorts was performed on displays with only a few input shorts, typically five or less. The time consuming nature of the repair process was due to two factors: first, the input short must be found by manually probing the shorted pins and measuring the resistance between the probes while the probes are traced through the display and second, the laser itself must be positioned manually. These factors suggested the binning approach that was adopted: displays with a few shorts were evaluated, repaired, and passed along to the subsequent steps of the testing sequence, while displays with more defects were set aside for failure analysis.

On all active matrix plates, select scanners were reworked with great success by the laser repair technique discussed above. *Displays with both sets of select scanners working properly were achieved.* Again, displays with the fewest select scanner problems were reworked first; displays with many select scanner problems were set aside for failure analysis.

As previously mentioned, testing of the data scanners is a time consuming process with our test system. Therefore, our approach was to randomly select about 5% of the lower and about 5% of the upper data scanners for testing, so permitting a manageable test time for the volume of displays to be tested. On average, we found more data scanner failures than select scanner failures, expected since the data scanner design is more complex.

Although nearest neighbor data scanner repair is most useful when all data scanners are tested, we did attempt laser repair on a subset of the data scanners tested. As before, the inclusion of laser sites allowed for highly successful nearest-neighbor shorting where appropriate. In the case of numerous failures, nearest-neighbor shorting was done only on displays with both select scanners working and in areas with only a few data scanner failures. This procedure allows isolation of completely functional areas within a display.

A comparison of the active matrix plates after metallization and after full processing indicated that "back-end" display processing, including passivation, does *not* add shorts, select scanner faults, or data scanner faults. In summary, testing of active matrix plates demonstrated:

- Both sets of select scanners were found to be operational after laser repair
- Nearest-neighbor shorting of data scanners was successful
- Large areas of the display were electrically functional after repairs
- Back-end display processing did not introduce input shorts, select scanner failures, or data scanner failures.

7.2.3 Assembled Displays

7.2.3.1 Test Procedures

Assembled displays are tested using the same sequence as described for fully processed active matrix plate testing in Section 7.2.2.3. Essentially no rework of fully assembled displays is possible; a test flow that accurately depicts this problem can be constructed by shading the remaining Rework box in Figure 7-4.b.

Rework for significant shorts is now impossible due to the presence of the top plate and liquid crystal material. The only shorts that can be cleared are trivial ones located at the input pins. These can be cleared since the bottom plate, upon which the display pins reside, is not completely covered by the top plate. However, pin-to-pin shorts are rare.

Test-and-repair of select and data scanners is also not possible with assembled displays, because of the presence of the top plate and associated assembly epoxy. The only tests still possible are the built-in tests of the select and data scanners that are available at the pins. Hence, while no repair can be accomplished, testing can still be used to determine if assembly destroyed functioning circuits. Currently, the built-in self test capabilities of the display are used to monitor for failures introduced during the assembly process.

Because of the restrictions on electrical testing and the inability to do significant repairs in the finished state, the design and test strategies adopted proved their worth. Key aspects of our approach to design and test were:

- Inclusion of structures to test all critical circuits separately
- Built-in redundancy to improve select scanner yield

- Testing early in the fabrication process before display assembly
- Monitoring the assembly process through built-in-self-testing capabilities.

7.2.3.2 Results

Electrical testing of fully assembled displays yielded results very similar to those obtained from the active matrix plates after metallization. *In general, the display assembly process did not adversely affect the active matrix plate.* In particular, no input shorts or select scanner failures were introduced in 80% of the assembled displays.

7.3 Optical Testing

As described in a previous report, WL-TR-95-1163, the underlying circuit architecture of the 1280 x 1024 display forms the basis for a family of displays of differing physical size and resolution. Two displays from this family of devices were optically tested. Hence, we can draw some conclusions from the combined measurements taken from the 1280 x 1024 displays and from a lower resolution derivative containing a smaller pixel.

7.3.1 Test Procedures

Optical testing of the assembled displays is done with the set-up illustrated schematically in Figure 7-7. Mounted on an optical bench, the apparatus has appropriate fixtures to hold the light valve in place. The optical measurements are done with a Photo Research SpectraScan PR-704 spectrophotometer with a 2° acceptance angle. An important consideration is the regulation on the tungsten light source so that numerous measurements can be taken over time. The display is electrically driven by a specially designed system.

The two optical quantities of greatest interest were measured: transmission (T) and full-field contrast ratio (CR). The transmission measurement was obtained using a three-step process: (1) measure transmission of the system without the light valve, (2) measure transmission of the system with light valve but without entrance and exit polarizers, and (3) measure transmission of the system with light valve and with entrance and exit polarizers. The contrast ratio measurement is a

full-field measurement; that is to say, light transmission is measured in two steps: (1) with all pixels driven black and (2) with all pixels driven white. CR measurements were obtained in both direct and projected viewing modes.

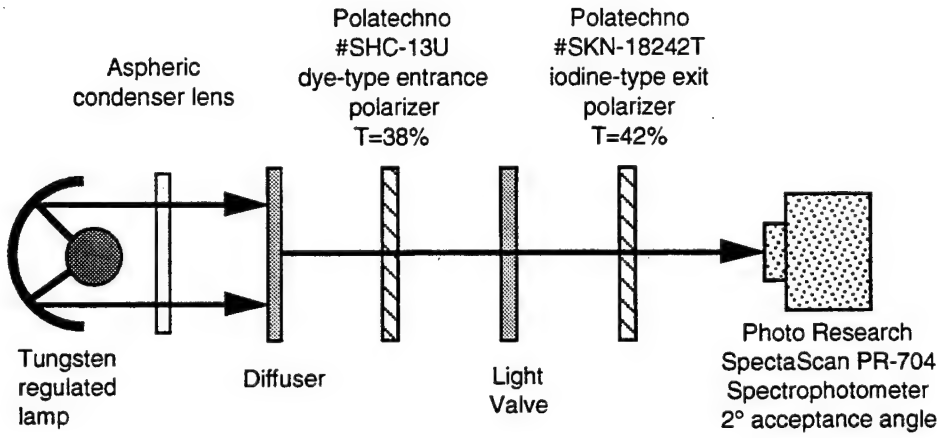


Figure 7-7. Optical test set-up.

7.3.2 Results

The results of optical testing are summarized in Table 7-1 for the two types of displays evaluated. The numbers represent typical measured values. Taking into account the transmission of components in the optical path—85% for the lens, 95% for the prism, 84% for the exit polarizer—2.3 Mlux is passed through the light valve in the projection system. The lower contrast ratio for the projection system is due to a light acceptance angle of about 10° versus the 2° acceptance angle of the spectrophotometer.

For a 37-μm pixel and an aperture greater than 50%, the 16% transmission is about the maximum to be expected. The 60:1 contrast ratio is sufficient for application in a projection system, keeping in mind that contrast ratio can be sacrificed to increase the aperture for projectors.

Table 7-1. Summary of optical measurements.

		1280x1024	Display #2
T(%)	no polarizers	47	29
T(%)	polarizers	16	10
T(%)	projection	n.a.	10.5
CR	direct view	60:1	90:1
CR	projection	n.a.	40:1

At the time of the writing of this report, Sarnoff continues to monitor both contrast ratio and transmission of newly manufactured light valves to establish production limits for these parameters. As contrast ratio and transmission improve, we plan to expand our optical testing to incorporate studies of the light valve's performance with respect to gray scale uniformity, light leakage, and reverse light sensitivity.

APPENDIX

ACTIVE MATRIX LIQUID CRYSTAL DISPLAY

GENERAL DESCRIPTION

The SRI020994 is a monochrome liquid crystal display with spatial resolution of 1280 horizontal pixels by 1024 vertical pixels. Data is input to the display via sixteen analog video channels. Integrated into the display is circuitry to perform the vertical/horizontal scan functions and provide required amplification and level shifting of the analog data.

FEATURES

37μ x 37μ Pixel ----> 2.4 Inch Display Diagonal
High Spatial Resolution (1280 x 1024)
Low Voltage Analog Video (0V to 5V)
Five Volt Digital Signals
Fifty-eight Pin Interface
Built-In Scanners
Electrical Test Ports For Production Testing

APPLICATIONS

Projectors

ABSOLUTE MAXIMUM RATINGS

Power Supplies	
|±VDD - GND|	+5.5V
|±VCC - GND|	+16.5V
Digital Input Voltage - GND	+5.5V
Analog Video Voltage - GND	+5.5V
Power Dissipation	500 mW
Storage Temperature	-50 to +85 Degrees C
Operating Temperature	0 to +50 Degrees C

System Description

A functional block diagram of the SRI020994 appears in Figure One. Data enters the display via a sixteen channel analog buss connecting to the input MULTIPLEXER. When enough data to service one horizontal display line has been sampled, this data is passed from the SAMPLE/HOLD block to the DATA DRIVER, freeing the MULTIPLEXER to input another line worth of data. An analog pipeline is thus formed between the SAMPLE/HOLD and the DATA DRIVER. The DATA DRIVER forces an appropriate analog voltage onto each vertical display line. The forced voltage differs from the raw analog input in a manner determined by the signals

RAMP, DATARAMP1, and DATARAMP2. These signals control amplification and level shifting of the raw analog data to provide waveforms suitable for driving the liquid crystal pixel array. Timing for the operations just described is provided by the TIMING block which also controls vertical scanning of the display by supplying the necessary signals to the SELECT scanner.

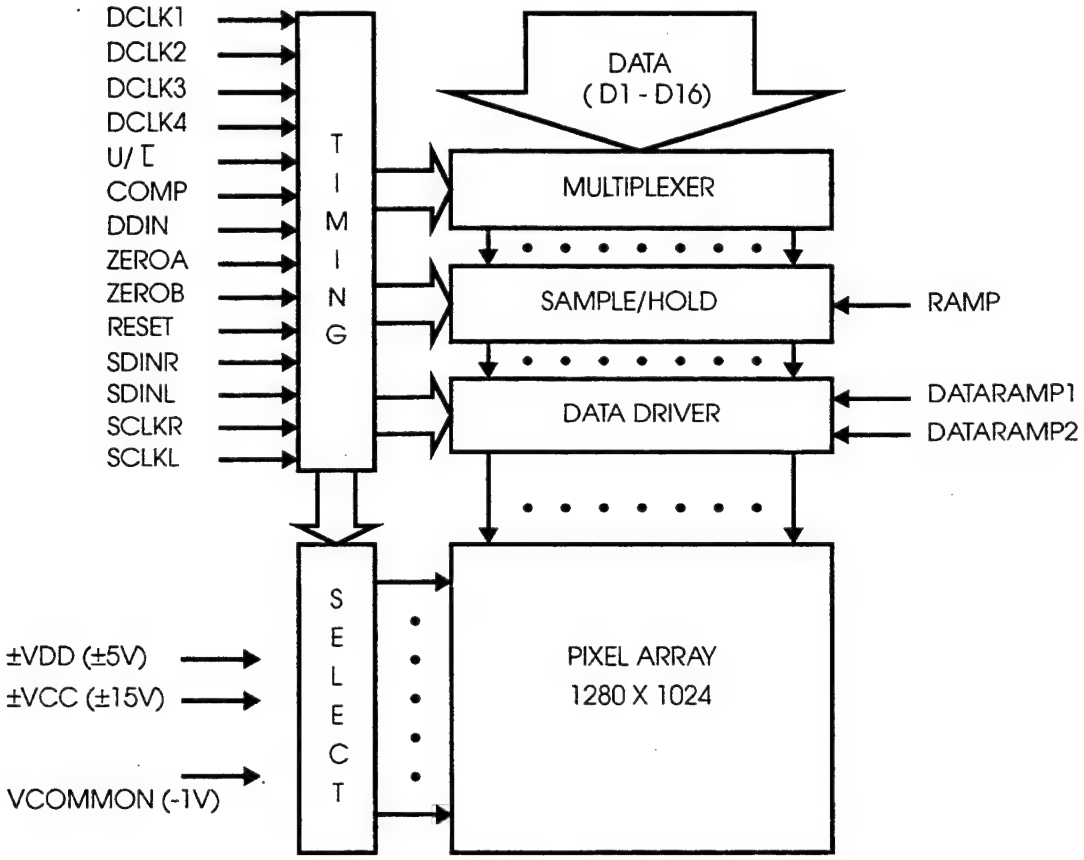


Figure One Functional Block Diagram

Fourteen timing inputs, DCLK1 - DCLK4, U/D, COMP, DDIN, ZEROA, ZEROB, RESET, SDINR, SDINL,SCLKR and SCLKL, properly sync the horizontal and vertical scanning of the display. Four supplies with nominal values of ±5V and ±15V provide operating power. RAMP is a linear ramp covering the span between ground (0V) and +VDD. DATARAMP1 and DATARAMP2 are linear ramps with settable endpoints nominally in the range of -7V to +5V. A potential is applied to the display common plane through input VCOMMON.

ELECTRICAL CHARACTERISTICS

(0 degrees C < T_A < 50 degrees C)

PARAMETERS	MIN	TYP	MAX	UNITS	COMMENTS
DC CHARACTERISTICS					
Supply Voltage					
|±VDD|	4.75	5	5.25	V	
|±VCC|	14.25	15	15.75	V	
Supply Current					Estimated dynamic + quiescent current
I_{+VDD}		4		mA	
I_{-VDD}		-8		mA	
I_{+VCC}		12		mA	
I_{-VCC}		-8		mA	
Digital Input Levels					Applies to U/D, COMP, DDIN, ZEROA, ZEROB,
V_{IH}	4.5			V	RESET, SDINR, SDINL, SCLKR & SCLKL
V_{IL}			0.5	V	Inputs assume CMOS drivers
Data Clocks					Applies to DCLK1 - DCLK4
V_{IH}	14.5			V	
V_{IL}			-4.5	V	
Analog Video	0.0		5.0	V	Applies to D1 - D16

ELECTRICAL CHARACTERISTICS

(0 degrees C < T_A < 50 degrees C)

PARAMETERS	MIN	TYP	MAX	UNITS	COMMENTS
DC CHARACTERISTICS					
Ramp Endpoints					**Adjustable for DATARAMP1 & DATARAMP2**
RAMP					
VL	-.5			V	Low level
VH			+5.5	V	High level
DATARAMPX					Applies to DATARAMP1 & DATARAMP2
VHA	-1	-1	+5	V	High level A relative to GND
VHB	VHA	+5	+5	V	High level B relative to GND
VLA	-7	-1	-1	V	Low level A relative to GND
VLB	-7	-7	VLA	V	Low level B relative to GND
VCOMMON	-5	-1	5	V	Variable from -5V to +5V

ELECTRICAL CHARACTERISTICS

(0 degrees C < T_A < 50 degrees C)

PARAMETERS	MIN	TYP	MAX	UNITS	COMMENTS
AC CHARACTERISTICS					
SCLKX (CIN < 25pf)					Applies to SCLKR $ SCLKL
F_{SCLK}	56.3	62.5	73.7	KHz	Continuous scanning for 55 -72 Hz frame rate
TR_{SCLK}			20	nS	10% to 90%
TF_{SCLK}			20	nS	90% to 10%
SDINX (CIN < 25pf)					Applies to SDINR $ SDINL
TS_{SDIN}	0			nS	
TH_{SDIN}	0			nS	
TR_{SDIN}			20	nS	10% to 90%
TF_{SDIN}			20	nS	90% to 10%
DCLKX (CIN < 60pf)					Applies to DCLK1 - DCLK4
F_{DCLK}	1.2	1.4	1.6	MHz	$F_{DCLK} = 22 X F_{SCLK}$
TR_{DCLK}			20	nS	10% to 90%
TF_{DCLK}			20	nS	90% to 10%
TS_{VIDEO}	1.2	1.4	1.6	µS	$TS_{VIDEO} = 2/F_{DCLK}$
DDIN (CIN < 25pf)					
TS_{DDIN}	300			nS	
TH_{DDIN}	0			nS	
TR_{DDIN}			5	nS	10% to 90%
TF_{DDIN}			5	nS	90% to 10%
DX (CIN < 50pf)					Applies to D1 - D16
TS_D		136		nS	$TS_D + TH_D = 1/(4 X F_{DCLK})$
TH_D		45		nS	
TR_D			5	nS	10% to 90%
TF_D			5	nS	90% to 10%

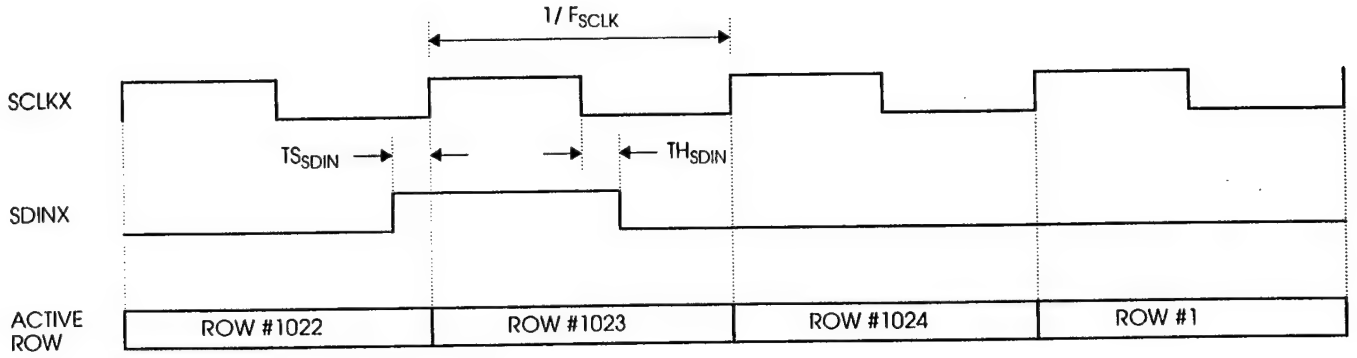
ELECTRICAL CHARACTERISTICS

(0 degrees C < T_A < 50 degrees C)

PARAMETERS	MIN	TYP	MAX	UNITS	COMMENTS
AC CHARACTERISTICS					
RAMP					
T_{RAMP}		7		µS	Ramping time
TR_{RAMP}			500	nS	
CIN		300		pf	
DATARAMPX					Applies to DATARAMP1 & DATARAMP2
$T_{DATARAMP}$		7		µS	Ramping time
$TR_{DATARAMP}$			500	nS	10% to 90%
$TF_{DATARAMP}$			500	nS	90% to 10%
CIN		13		nf	
U/$\overline{D}$ (CIN < 50pf)					
$F_{U/\overline{D}}$		31.25		KHz	$F_{U/\overline{D}} = F_{SCLK}/2$
$TR_{U/\overline{D}}$			20	nS	10% to 90%
$TF_{U/\overline{D}}$			20	nS	90% to 10%
ZEROX (CIN < 50pf)					Applies to ZEROA & ZEROB
T_{ZERO}		3.0		µS	
T_{LAP}		0.5		µS	
TR_{ZERO}			20	nS	10% to 90%
TF_{ZERO}			20	nS	90% to 10%
COMP (CIN < 25pf)					
T_{COMP}		8.5		µS	
TR_{COMP}			20	nS	10% to 90%
TF_{COMP}			20	nS	90% to 10%
RESET (CIN < 25pf)					
T_{RESET}		3.0		µS	
TR_{RESET}			20	nS	10% to 90%
TF_{RESET}			20	nS	90% to 10%

TIMING DIAGRAMS

VERTICAL SCAN TIMING



NOTES: 1) SCLKX must run continuously.

2) SDINX repeats every 1024 SCLK cycles for continuous scanning.

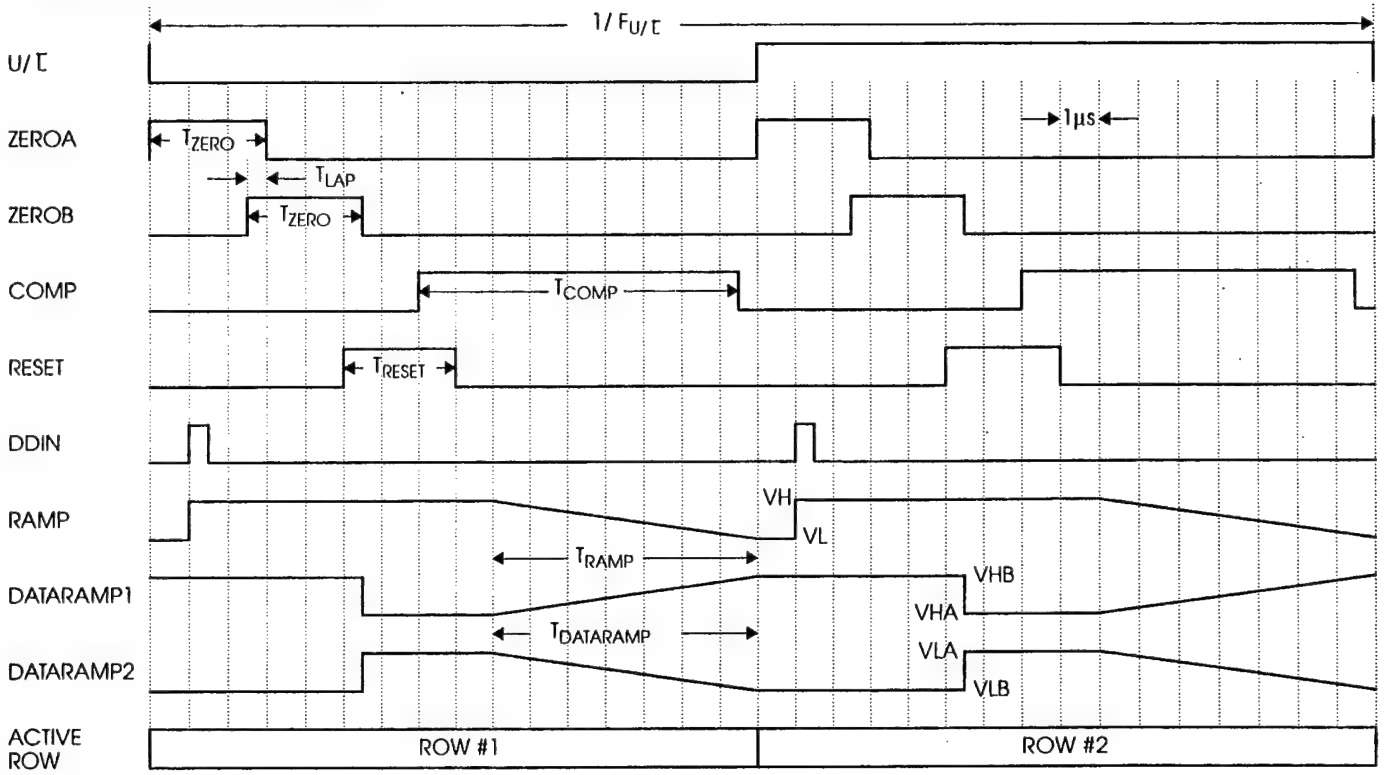
3) Noncontinuous vertical scanning is possible but not presently specified.

4) Row #1 is active (receives data) during the third SCLKX cycle after the occurrence of SDINX.

5) SCLKX & SDINX represent SCLKR/SCLKL & SDINR/SDINL.

TIMING DIAGRAMS

HORIZONTAL SCAN TIMING



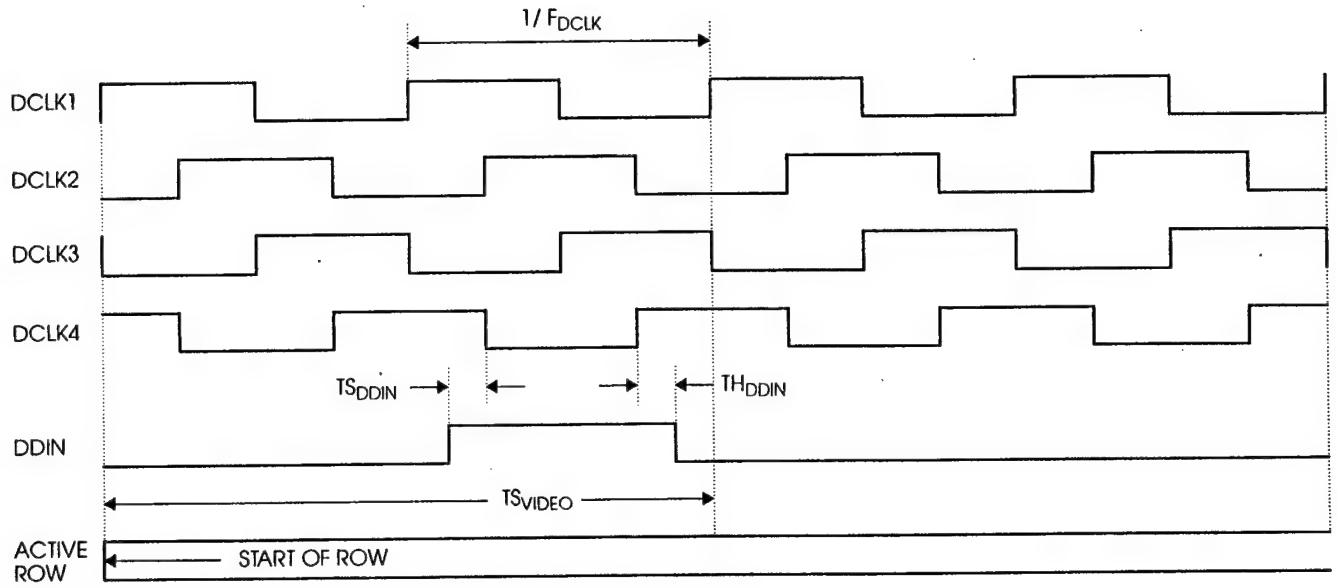
NOTES: 1) $F_{U/D} = F_{SCLK}/2$.

2) Timing diagram is to scale for F_{SCLK} = 62.5 KHz.

3) U/D synchronizes horizontal and vertical scanning. DDIN synchronizes the transmission of video data.

TIMING DIAGRAMS

HORIZONTAL SCAN TIMING (DDIN and Data Clock Detail)



NOTES: 1) DCLK1 - DCLK4 must run continuously.

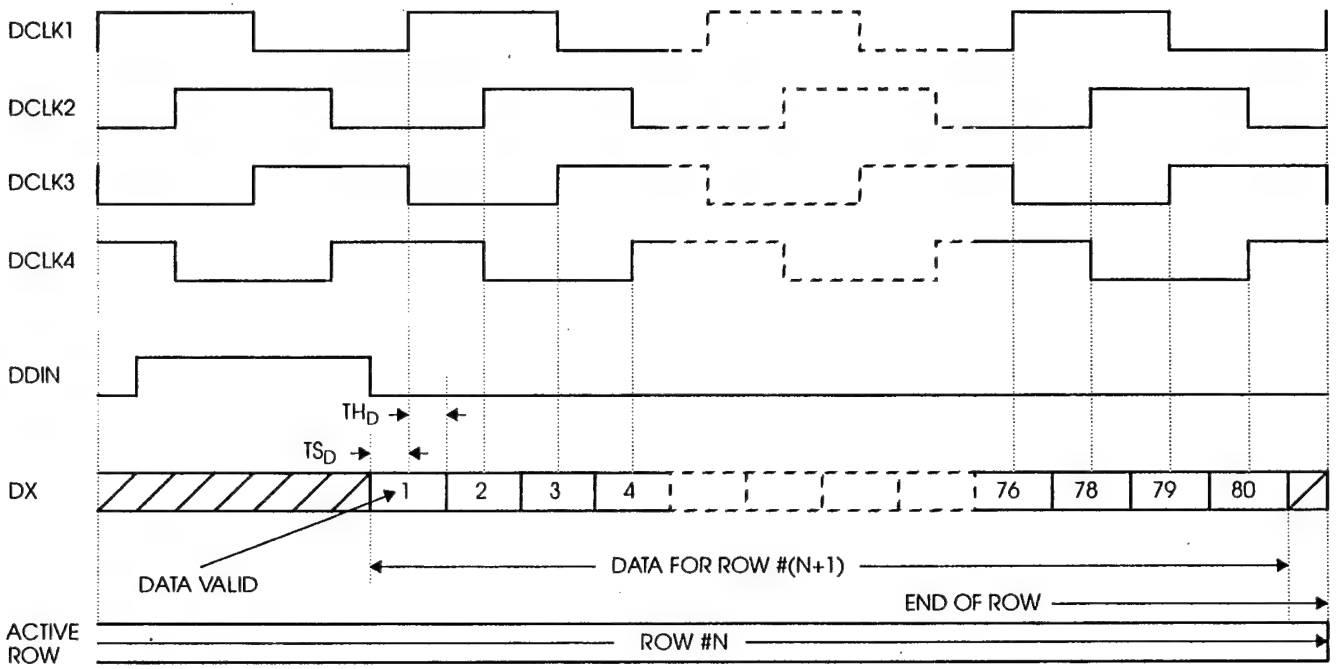
2) $F_{DCLK} = 22 \times F_{SCLK}$.

3) TS_{VIDEO} locates the first DCLK1 rising edge after the occurrence of DDIN. Data transmission is initiated on this edge.

4) DCLKX rising edge must occur before falling edge of complementary clock. DCLK1 and DCLK3 are complementary as are DCLK2 and DCLK4.

TIMING DIAGRAMS

HORIZONTAL SCAN TIMING (Data Clock and Analog Video Detail)



NOTES: 1) DX represents D1 - D16.

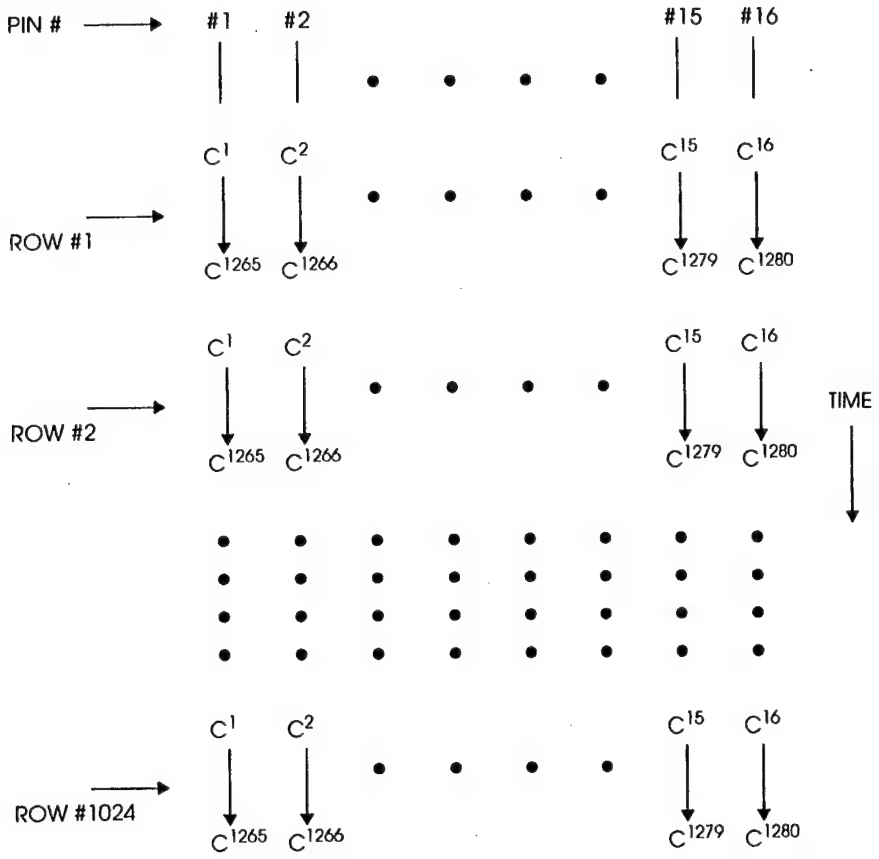
2) D1 - D16 are sixteen analog video channels.

3) Each analog channel provides data for 80 columns of the display. Sixteen channels are required to service all 1280 columns.

4) Data for row #(N+1) is provided to the display while row #N is active.

TIMING DIAGRAMS

DATA ORDER



NOTES

1) There are a total of sixteen DATA pins.

2) Each DATA pin services 80 columns of pixels.

3) The diagram to the left illustrates the data ordering for the sixteen pins.

4) C^Y indicates the data for column Y.

5) Within a row data is received by the display in a single burst of 1280 analog sample & held values. Each DATA pin transmits 80 of these values.

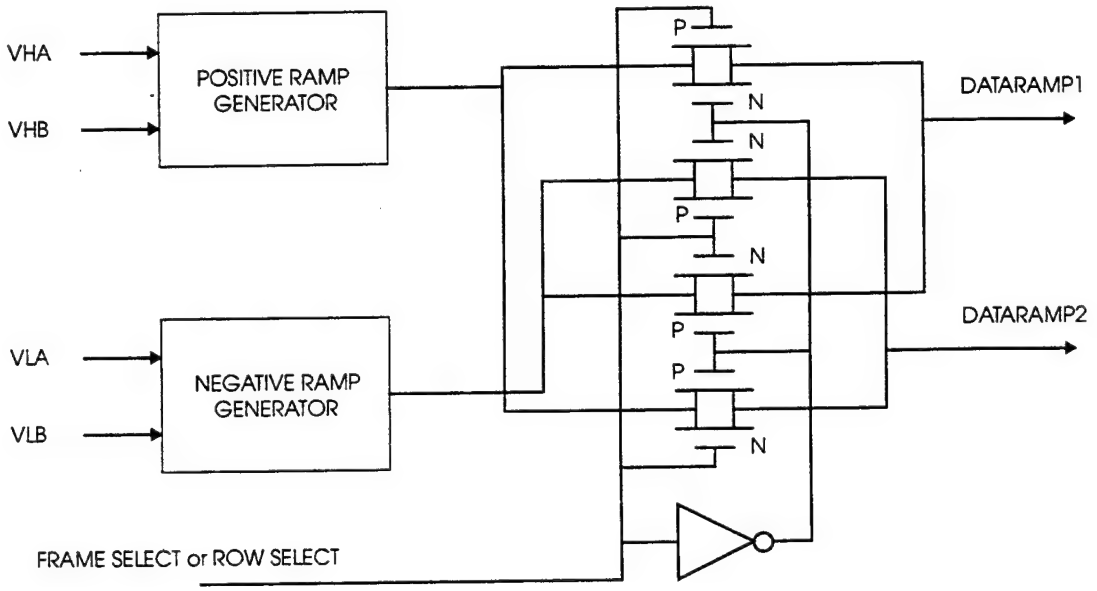
OPTICAL CHARACTERISTICS

(0 degrees C < T_A < 50 degrees C)

PARAMETERS	MIN	TYP	MAX	UNITS	COMMENTS
MISCELLANEOUS CHARACTERISTICS					
Pixel Size					
X		37		µ	
Y		37		µ	
Pixel Aperture		50		%	
Pixel Transmission		15		%	
Contrast Ratio		60:1			Full field measurement

RECOMMENDED OPERATING PROCEDURES

DATARAMPX GENERATION



NOTES

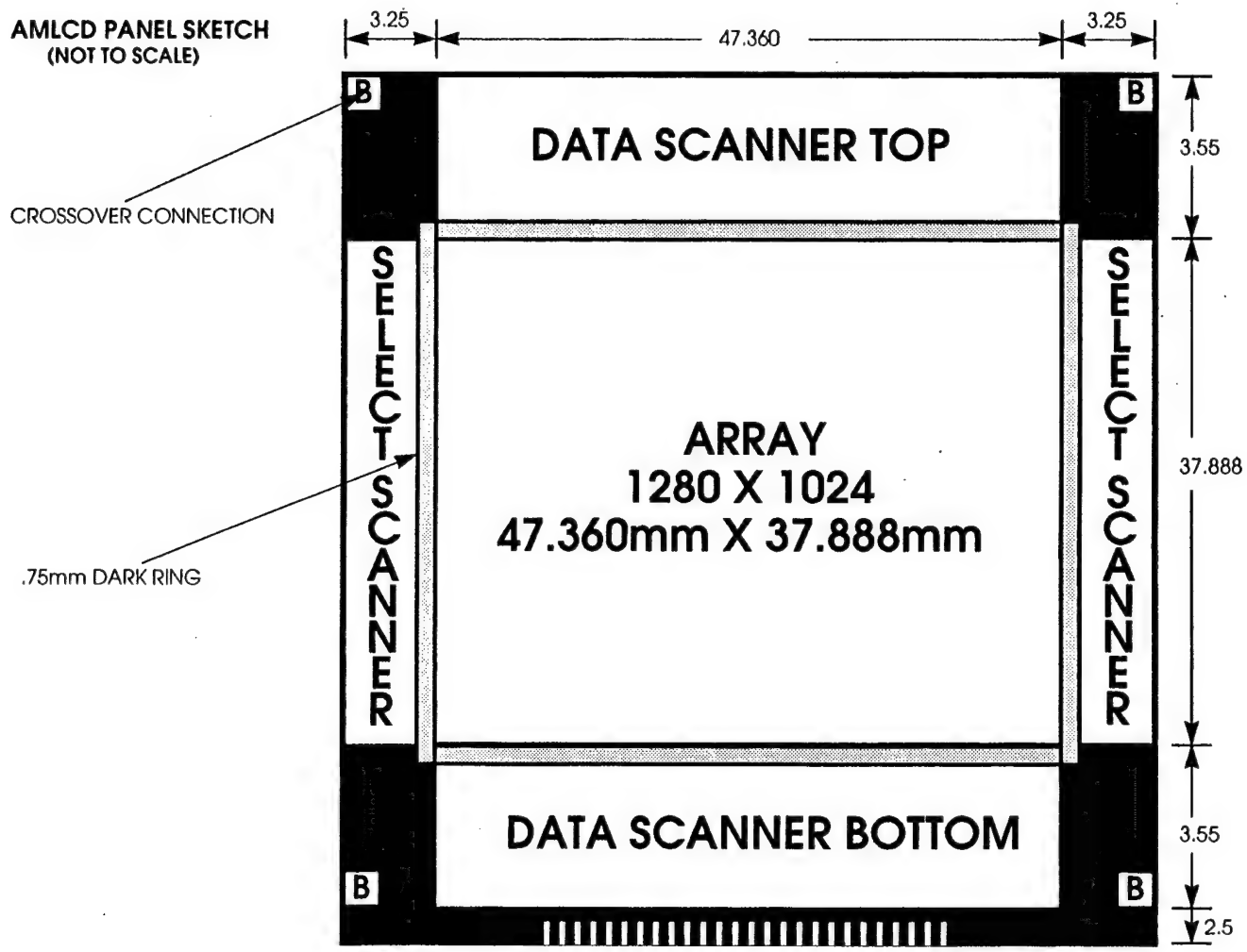
1) The objective of using this circuit to generate DATARAMP1 and DATARAMP2 is to guarantee that the input ramps have identical behavior.

2) VHA, VHB, VLA, and VLB are endpoint adjustments for the ramps.

3) FRAME SELECT permits DATARAMP1 and DATARAMP2 to exchange roles after every frame. This implements column inversion.

4) ROW SELECT permits DATARAMP1 and DATARAMP2 to exchange roles after every row. This implements column inversion combined with row inversion.

AMLCD PANEL SKETCH
(NOT TO SCALE)



PIN ASSIGNMENTS

Pin #	Name	Input	Output	Function
1	VCOMMON	X		Common Plane Voltage
2	DCLK1	X		Data Clock
3	DCLK2	X		Data Clock
4	DDIN	X		Data Sync
5	D2	X		Data
6	D6	X		Data
7	D10	X		Data
8	D14	X		Data
9	ZEROA	X		Horizontal Timing
10	DATARAMP2	X		Drive Ramp
11	RAMP	X		Signal Ramp
12	TC-IN	X		Temperature Compensation In
13	U/$\overline{L}$	X		Horizontal Timing
14	COMP	X		Horizontal Timing
15	RESET	X		Horizontal Timing
16	+VDD	X		+5V Supply
17	+VCC	X		+15V Supply
18	-VDD	X		-5V Supply
19	-VCC	X		-15V Supply
20	D1U		X	Data Scanner Test Out
21	SDINL	X		Vertical Scan Sync
22	SCLKL	X		Vertical Scan Clock
23	DATARAMP1	X		Drive Ramp
24	D1L		X	Data Scanner Test Out
25	D13	X		Data
26	D9	X		Data
27	D5	X		Data
28	D1	X		Data
29	STL		X	Select Scanner Test Out
30	DCLK1	X		Data Clock
31	DCLK2	X		Data Clock
32	DCLK3	X		Data Clock
33	DCLK4	X		Data Clock
34	STR		X	Select Scanner Test Out
35	D3	X		Data
36	D7	X		Data
37	D11	X		Data
38	D15	X		Data
39	D2U		X	Data Scanner Test Out
40	DATARAMP1	X		Drive Ramp
41	SCLKR	X		Vertical Scan Clock
42	SDINR	X		Vertical Scan Sync
43	TC-OUT		X	Temperature Compensation Out

PIN ASSIGNMENTS (CONTINUED)

Pin #	Name	Input	Output	Function
44	-VCC	X		-15V Supply
45	-VDD	X		-5V Supply
46	+VCC	X		+15V Supply
47	+VDD	X		+5V Supply
48	RAMP	X		Signal Ramp
49	DATARAMP2	X		Drive Ramp
50	ZEROB	X		Horizontal Timing
51	D16	X		Data
52	D12	X		Data
53	D8	X		Data
54	D4	X		Data
55	D2L		X	Data Scanner Test Out
56	DCLK4	X		Data Clock
57	DCLK3	X		Data Clock
58	VCOMMON	X		Common Plane Voltage

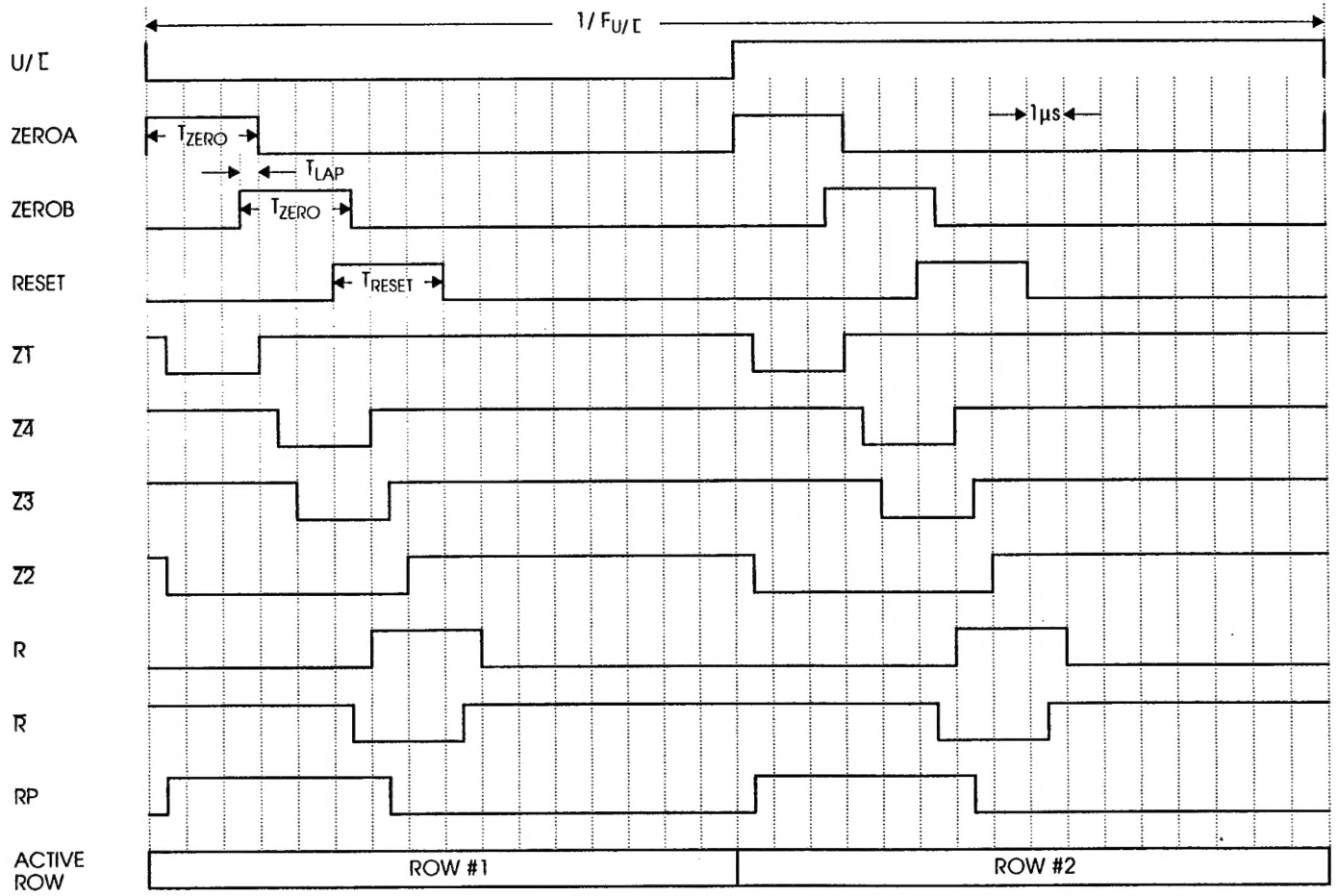
Note: Pins 20,24,39, & 55 are data scanner test outputs and should be tied to VCOMMON during normal operation.

Note: Pins 29 & 34 are select scanner test outputs and should be tied to +VDD during normal operation.

Note: Pin 12 is a temperature compensation input and should be tied to +VDD when not being used.

INTERNAL TIMING DIAGRAMS

HORIZONTAL SCAN TIMING



INTERNAL TIMING DIAGRAMS

HORIZONTAL SCAN TIMING